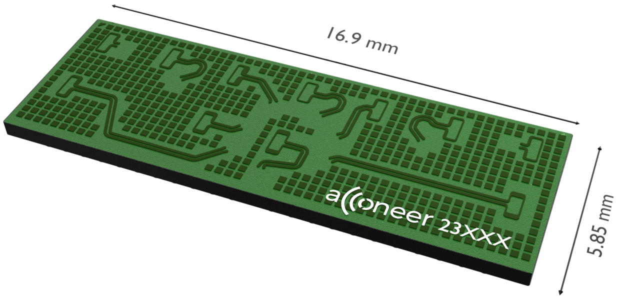
A212-003 Pulsed Coherent Radar (PCR)

1. Applications

- **Addressable applications**
    - Presence detection.
    - People tracking and people counting.
    - Fall detection.
    - Classification. Human vs pet or human by size.
    - Heartbeat monitoring, breathing and sleep quality.
    - Gesture control.
    - Distance measurement in multiple angles.
    - Material classification.

2. Features

- **Accurate distance ranging and movements**
    - Measures absolute range up to 25m.
    - Absolute accuracy in mm.
    - Relative accuracy in µm.
    - Possible to recognize movement and gestures for several objects.
    - Support continuous and single sweep mode.
    - System Field of View (FoV) of 108° along the H-plane and 76° along the E-plane.
- **Easy integration**
    - 60 GHz Pulsed Coherent Radar.
    - Integrated 32-bit RISC-V Processor, 286MHz.
    - RF front-end and Antenna-in-Package; 3Tx4Rx.
    - 5.85 mm x 16.90 mm x 0.90 mm fcCSP, 0.65 mm pitch.
    - Can be integrated behind plastic or glass without any need for a physical aperture.



- Single reflowable component.
- 1.8 V single power supply, enable with Power on Reset (PoR).
- 1.8 V or 3.3 V I/O interface power supply.
- Clock input for 26 MHz crystal.
- 32 kHz internal oscillator for low-power operation.
- (Q)SPI interface for data transfer, up to 50 MHz (Q)SPI clock support.
- Interrupt support.
- **Qualification and standards**
    - JEDEC (JESD47).
    - HBM +-1.5kV, CDM +-500V.
    - RoHS, REACH.
- **Compliance (target)**
    - Certifiable in EU, FCC, JP and all countries that have adapted either EU or FCC regulatory standards.

3. Overview

The A212 is a 60 GHz, multiantenna radar system based on PCR technology. The device sets new benchmarks for angular resolution, accuracy and distance resolution.

The A212 60 GHz radar system is optimized for high precision and low power, delivered as a one package solution with an integrated MCU based on a 32-bit, 286-MHz RISC-V processor, an RF front-end, and 3Tx4Rx antennas. This will enable easy integration into any device.

The A212 is based on leading-edge, patented pulsed coherent radar technology with pico-second time resolution. The sensor can measure up to 25 meters, with the actual measurable distance being dependent on object size, shape, and dielectric properties. For example:

- Human presence detection up to 12 meters with lens-free utilization.
- Heartbeat monitoring measurement up to 3 meters without lens utilization.
- Breathing and sleep measurements up to 5 meters without lens utilization.

The A212 60 GHz radar remains uncompromised by any natural source of interference, such as noise, dust, color and direct or indirect light.

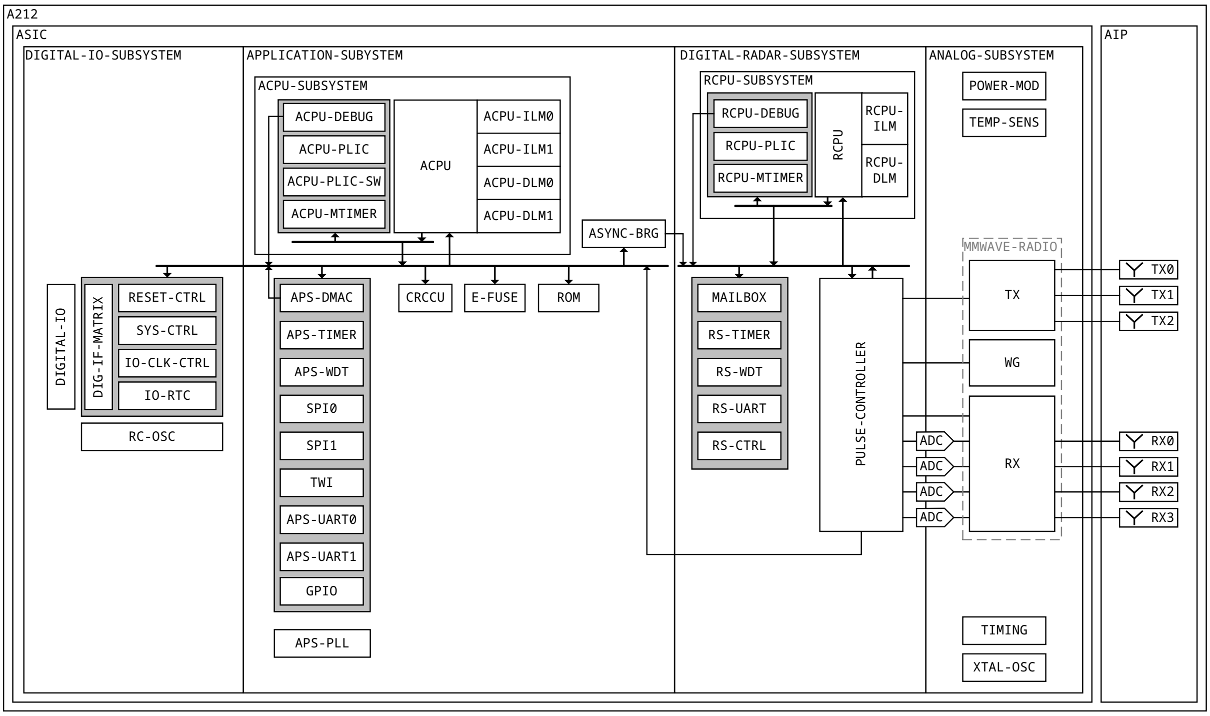


Figure 1: A212 functional block diagram.

For further information see Section 10.

4. Ordering information

Table 1: Ordering information.

Part number	Package	Nominal size	Component container	Quantity
A212-003-TY	fcCSP53	16.90 x 5.85 x 0.90 mm	Tray	210 pieces / tray
A212-003-T&R	fcCSP53	16.90 x 5.85 x 0.90 mm	Tape and reel	3000 pieces / reel

5. Revision history

Table 2: Revision history.

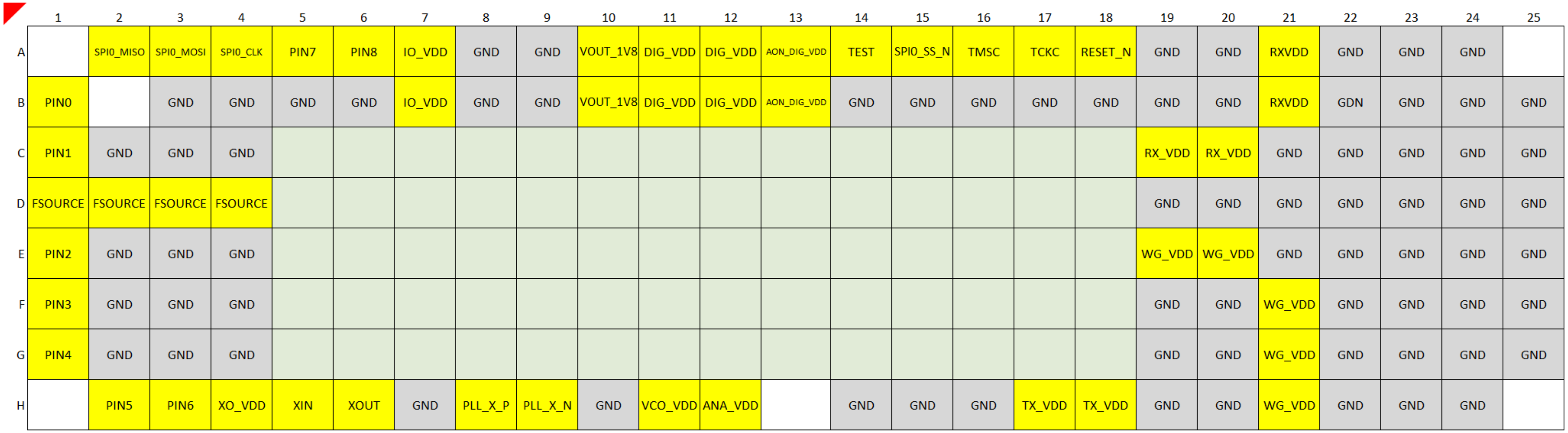
Revision	Change description
v0.18	• First public revision.

6. Contents

7. Pin configurations and functions

7.1. Pin configuration

Figure 2 below shows the A212 pin configuration as seen from the top of the package. For the antenna configuration please refer to Section 10.1.10.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A		SPI0_MISO	SPI0_MOSI	SPI0_CLK	PIN7	PIN8	IO_VDD	GND	GND	VOUT_1V8	DIG_VDD	DIG_VDD	AON_DIG_VDD	TEST	SPI0_SS_N	TMSC	TCKC	RESET_N	GND	GND	RXVDD	GND	GND	GND	
B	PIN0		GND	GND	GND	GND	IO_VDD	GND	GND	VOUT_1V8	DIG_VDD	DIG_VDD	AON_DIG_VDD	GND	GND	GND	GND	GND	GND	GND	RXVDD	GDN	GND	GND	GND
C	PIN1	GND	GND	GND															RX_VDD	RX_VDD	GND	GND	GND	GND	GND
D	FSOURCE	FSOURCE	FSOURCE	FSOURCE															GND	GND	GND	GND	GND	GND	GND
E	PIN2	GND	GND	GND															WG_VDD	WG_VDD	GND	GND	GND	GND	GND
F	PIN3	GND	GND	GND															GND	GND	WG_VDD	GND	GND	GND	GND
G	PIN4	GND	GND	GND															GND	GND	WG_VDD	GND	GND	GND	GND
H		PIN5	PIN6	XO_VDD	XIN	XOUT	GND	PLL_X_P	PLL_X_N	GND	VCO_VDD	ANA_VDD		GND	GND	GND	TX_VDD	TX_VDD	GND	GND	WG_VDD	GND	GND	GND	

Figure 2: A212 pin configuration, top view.

Table 3: A212 pin assignment.

Pin name	Ball coordinates
`GND`	A8:A9, A19:A20, A22:A24, B3:B6, B8:B9, B14:B20, B22:B25, C2:C4, C21:C25, D19:D25, E2:E4, E21:E25, F2:F4, F19:F20, F22:F25, G2:G4, G19:G20, G22:G25, H7, H10, H14:H16, H19:H20, H22:H24
`IO_VDD`	A7, B7
`DIG_VDD`	A11, A12, B11, B12
`ANA_VDD`	H12
`XO_VDD`	H4

Pin name	Ball coordinates
`VCO_VDD`	H11
`RX_VDD`	A21, B21, C19, C20
`TX_VDD`	H17, H18
`WG_VDD`	E19, E20, F21, G21, H21
`VOUT_1V8`	A10, B10
`AON_DIG_VDD`	A13, B13
`FSOURCE`	D1, D2, D3, D4
`RESET_N`	A18
`SPI0_SS_N`	A15
`SPI0_CLK`	A4
`SPI0_MISO`	A2
`SPI0_MOSI`	A3
`PIN0`	B1
`PIN1`	C1
`PIN2`	E1
`PIN3`	F1
`PIN4`	G1
`PIN5`	H2
`PIN6`	H3
`PIN7`	A5
`PIN8`	A6
`TMSC`	A16
`TCKC`	A17
`TEST`	A14

Pin name	Ball coordinates
`XIN`	H5
`XOUT`	H6
`PLL_X_P`	H8
`PLL_X_N`	H9

7.2. Pin functions

Table 4 provides the description of the supply pins, including nominal supply values and related domains.

Table 4: A212 supply pins.

Pin name	Pin type	Domain	Value	Comments
`GND`	ground	A212	0V	
`IO_VDD`	supply input	DIGITAL-IO, POWER-MOD	1.8V / 3.3V	
`DIG_VDD`	supply input	POWER-MOD, DIOS, APS, DRS	1.8V	
`ANA_VDD`	supply input	ADC, TIMING	1.8V	
`XO_VDD`	supply input	XTAL-OSC	1.8V	
`VCO_VDD`	supply input	TIMING	1.8V	
`RX_VDD`	supply input	RX	1.8V	
`TX_VDD`	supply input	TX	1.8V	
`WG_VDD`	supply input	WG	1.8V	
`VOUT_1V8`	supply output	`DIG_VDD`, `ANA_VDD`, `XO_VDD`, `VCO_VDD`, `RX_VDD`, `TX_VDD`, `WG_VDD`	1.8V	Regulated 1.8V from `IO_VDD`. See Section 11.1.
`AON_DIG_VDD`	analog output	DIOS	1.1V	Used for connecting external decoupling.
`FSOURCE`	ground	E-FUSE	0V	Connect to solid ground.

Table 5: Digital I/O pins.

Pin name	Pin type	Pull capabilities	Alternate functions					Comments
RESET_N	input	PU(A)	RESET_N					
SPI0_SS_N	input(R)(D) / output(N)	PU(R)(D)(N) / PD	SPI0_SS_N(D)(N)	BOOT_SEL(R)				
SPI0_CLK	input(D) / output(N)	PU(D) / PD	SPI0_CLK(D)(N)					
SPI0_MOSI	input(D) / output(N)	PU(D) / PD	SPI0_MOSI(D)(N)					
SPI0_MISO	input(N) / output(D)	PU(D) / PD	SPI0_MISO(D)(N)					
PIN0	input(D) / output	PU(D) / PD	SPI0_IO2	GPIO0				
PIN1	input(D) / output	PU(D) / PD	SPI0_IO3	GPIO1				
PIN2	input / output	PU / PD		GPIO2	UART1_TX	LIN_TX		
PIN3	input / output	PU / PD	SPI1_SS_N	GPIO3	UART1_RX	LIN_RX	TWI_SCL	
PIN4	input / output	PU / PD	SPI1_CLK	GPIO4		LIN_CTRL	TWI_SDA	
PIN5	input(D) / output	PU / PD	SPI1_MOSI	GPIO5	UART0_CTS			
PIN6	input / output(D)	PU(D) / PD		GPIO6	UART0_TX(D)			
PIN7	input(D) / output	PU(D) / PD		GPIO7	UART0_RX(D)			
PIN8	input / output	PU / PD	SPI1_MISO	GPIO8	UART0_RTS			
TMSC	input / output	PU(R)(D)(N) / PD						
TCKC	input	PU(R)(D)(N) / PD						

(A): Always active.
(R): Behavior during reset.
(D): Behavior during/after DFU boot.
(N): Behavior during/after NVM boot.

PU: Pull-up.
PD: Pull-down

Table 6: A212 analog pins.

Pin name	Pin type	Function	Reference voltage	Comments
`TEST`	input	Reserved	1.1V	Connect to solid ground plane.
`XIN`	input	XTAL interface	1.1V	See Section 11.2.
`XOUT`	output	XTAL interface	1.1V	See Section 11.2.
`PLL_X_P`	input/output	Reserved	`ANA_VDD`	Connect to solid ground plane.
`PLL_X_N`	input/output	Reserved	`ANA_VDD`	Connect to solid ground plane.

8. Specifications

8.1. Absolute maximum ratings

Table 7 below shows the A212 absolute maximum ratings over the operating temperature range, on package. Note that the digital input pins are listed in Table 5.

Table 7: Absolute maximum ratings (on package).

Symbol	Parameter	Min	Max	Unit	Condition
V_{IO}	`IO_VDD` supply voltage rating	−0.5	3.8	V	
V_{DIG}	`DIG_VDD` supply voltage rating	−0.5	2.0	V	
V_{ANA}	`ANA_VDD` supply voltage rating	−0.5	2.0	V	
V_{XO}	`XO_VDD` supply voltage rating	−0.5	2.0	V	
V_{VCO}	`VCO_VDD` supply voltage rating	−0.5	2.0	V	
V_{RX}	`RX_VDD` supply voltage rating	−0.5	2.0	V	
V_{TX}	`TX_VDD` supply voltage rating	−0.5	2.0	V	
V_{WG}	`WG_VDD` supply voltage rating	−0.5	2.0	V	
V_{GPIO}	Digital inputs voltage rating	−0.5	V_{IO}+0.5	V	
V_{XIN}	`XIN` voltage	−0.5	V_{IO}+0.5	V	
T_j	Junction temperature	−40	125	°C	
T_{stg}	Storage temperature	−40	150	°C	

Stress beyond the limits listed in Table 7 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions or at any other conditions beyond those indicated under Section 8.3 is not recommended. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

8.2. Environmental sensitivity

Table 8: Environmental sensitivity.

Symbol	Parameter	Value	Unit	Standard
T_{reflow}	Reflow soldering temperature	260	°C	J-STD-020
`MSL`	Moisture sensitivity level	MSL3		JESD22-A113
$V_{ESD-CDM}$	ESD, Charge Device Model (CDM)	1000	V	JS-002, Class C3
$V_{ESD-HBM}$	ESD, Human Body Model (HBM)	2000	V	JS-001, Class 2
V_{LU}	Latch-up	PASS		JESD78, Class I

8.3. Recommended operating conditions

Table 9 below shows the A212 recommended operating conditions on package.

Table 9: Recommended operating conditions (on package).

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$V_{\mathtt{IO}}$	`IO_VDD` supply voltage - 3.3 V mode	2.97	3.3	3.63	V	
	`IO_VDD` supply voltage - 1.8 V mode	1.67	1.8	1.98	V	
$V_{\mathtt{DIG}}$	`DIG_VDD` supply voltage	1.67	1.8	1.98	V	
$V_{\mathtt{ANA}}$	`ANA_VDD` supply voltage	1.67	1.8	1.98	V	
$V_{\mathtt{XO}}$	`XO_VDD` supply voltage	1.67	1.8	1.98	V	
$V_{\mathtt{VCO}}$	`VCO_VDD` supply voltage	1.67	1.8	1.98	V	
$V_{\mathtt{RX}}$	`RX_VDD` supply voltage	1.67	1.8	1.98	V	
$V_{\mathtt{TX}}$	`TX_VDD` supply voltage	1.67	1.8	1.98	V	
$V_{\mathtt{WG}}$	`WG_VDD` supply voltage	1.67	1.8	1.98	V	
T_{op}	Ambient operating temperature	−40		85	°C	

8.4. Electrical specification

8.4.1. Digital IOs

Table 10: Electrical DC specifications (on package, $-40\ °C \le T_{op} \le 85\ °C$).

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IL}	Digital I/O low-level input voltage	−0.3		$0.10 \cdot V_{IO}$	V	
V_{IH}	Digital I/O high-level input voltage	$0.90 \cdot V_{IO}$		$V_{IO}+0.3$	V	
V_{OL}	Digital I/O low-level output voltage	0		0.4	V	
V_{OH}	Digital I/O high-level output voltage	$V_{IO}-0.4$		V_{IO}	V	
I_{OL}	Digital I/O low-level output current	4.56	7.8	12.4	mA	$V_{OL} = 0.4V$
I_{OH}	Digital I/O high-level output current	3.42	5.8	9.16	mA	$V_{OH} = V_{IO}-0.4V$
I_{IL}	Digital I/O low-level input current			<1	µA	
I_{IH}	Digital I/O high-level input current			<1	µA	
R_{PU}	Digital I/O internal pull-up resistor value	40		75	kΩ	
R_{PD}	Digital I/O internal pull-down resistor value	40		85	kΩ	
I_{IO}	IO_VDD supply current			1	mA	
I_{DIG}	DIG_VDD supply current			150	mA	
I_{ANA}	ANA_VDD supply current			60	mA	
I_{XO}	XO_VDD supply current			2	mA	
I_{VCO}	VCO_VDD supply current			11	mA	
I_{RX}	RX_VDD supply current			40	mA	
I_{TX}	TX_VDD supply current			25	mA	
I_{WG}	WG_VDD supply current			35	mA	
$V_{AON\_DIG\_VDD}$	AON_DIG_VDD output voltage	1.045	1.1	1.155	V	
V_{VOUT_1V8}	VOUT_1V8 output voltage	1.71	1.8	1.89	V	

Table 11: Electrical AC specifications (on package, $-40\ °C \le T_{op} \le 85\ °C$).

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$f_{op(IO)}$	Digital I/O output operating frequency	0		100	MHz	$C_L \le 2$ pF
$t_{w(IO)}$	Digital I/O positive and negative pulse width	6.25			ns	
V_{XIN}	XIN AC voltage amplitude		1.1	1.21	V_{pp}	
V_{XOUT}	XOUT AC voltage amplitude		1.1	1.21	V_{pp}	

8.5. Current consumption

Table 12: Total current consumption per sensor state (T_{op} = 25 °C, nominal supplies).

Symbol	Parameter	Typ	Unit	Condition
$I_{\texttt{sleep-ultra}}$	Current consumption, `SLEEP-ULTRA-DEEP` state	40	uA	
$I_{\texttt{sleep-deep}}$	Current consumption, `SLEEP-DEEP` state	46	uA	
$I_{\texttt{sleep-shallow}}$	Current consumption, `SLEEP-SHALLOW` state	0.28	mA	
$I_{\texttt{idle}}$	Current consumption, `IDLE` state	1.1	mA	
$I_{\texttt{processing}}$	Current consumption, `PROCESSING` state	33	mA	
$I_{\texttt{measure}}$	Current consumption, `MEASURE` state	174	mA	Profile 1, 2, 3, 5; PRF = 27.7 MHz.
$I_{\texttt{measure-p6}}$	Current consumption, `MEASURE` state	182	mA	Profile 6; PRF = 27.7 MHz
$I_{\texttt{full}}$	Current consumption, `FULL` state	192	mA	Profile 1, 2, 3, 5; PRF = 27.7 MHz.
$I_{\texttt{full-p6}}$	Current consumption, `FULL` state	200	mA	Profile 6; PRF = 27.7 MHz

8.6. Power supply ripple

Table 13: Power supply ripple specifications (T_{op} = 25 °C).

Frequency [kHz]	Max Supply Ripple [mVpp]
50	30
100	30
200	15
300	15
500	12
750	7
1000	7
1500	5

8.7. RF specifications

Table 14: RF specifications (on package, T_{op} = 25 °C, nominal supplies).

Symbol	Parameter	Min	Typ	Max	Unit	Condition
f_{RF}	Operating frequency range	57		64	GHz	
$EIRP_{TX0}$	Peak EIRP, TX0 antenna		18.9		dBm	
$EIRP_{TX1}$	Peak EIRP, TX1 antenna		19.6		dBm	
$EIRP_{TX2}$	Peak EIRP, TX2 antenna		17.9		dBm	
DR_{RX}	RX dynamic range		50		dBFs	Per single IQ sample.
$BW_{-6dB,az}$	-6dB System Beam Width, azimuth plane(*)		108		deg	
$BW_{-6dB,el}$	-6dB System Beam Width, elevation plane(*)		76		deg	

(*): Using −6dB for the definition of $BW_{-6dB,az}$ and $BW_{-6dB,el}$ makes them comparable to HPBW figures for the Tx and Rx antennas.

Figure 3 shows the combined Base Radar-Loop Gain (Base RLG) of the system as a function of the azimuth and elevation angles, with contour lines every 3 dB, for the *conventional* beamforming setting of RSS. The dashed straight lines denote the $BW_{-6dB,az}$ and $BW_{-6dB,el}$ angles.

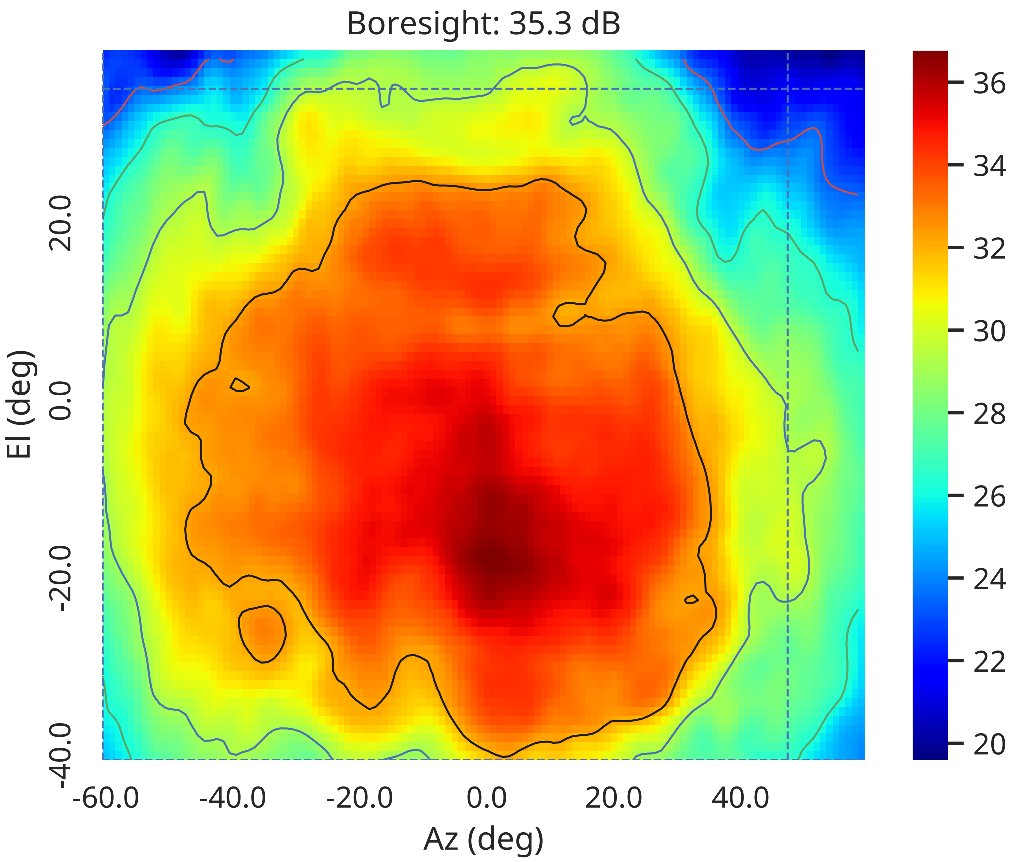


Figure 3: Combined Base Radar-Loop Gain (Base RLG) of all 12 channels in the system as a function of the azimuth and elevation angles (beamforming=conventional, profile=3).

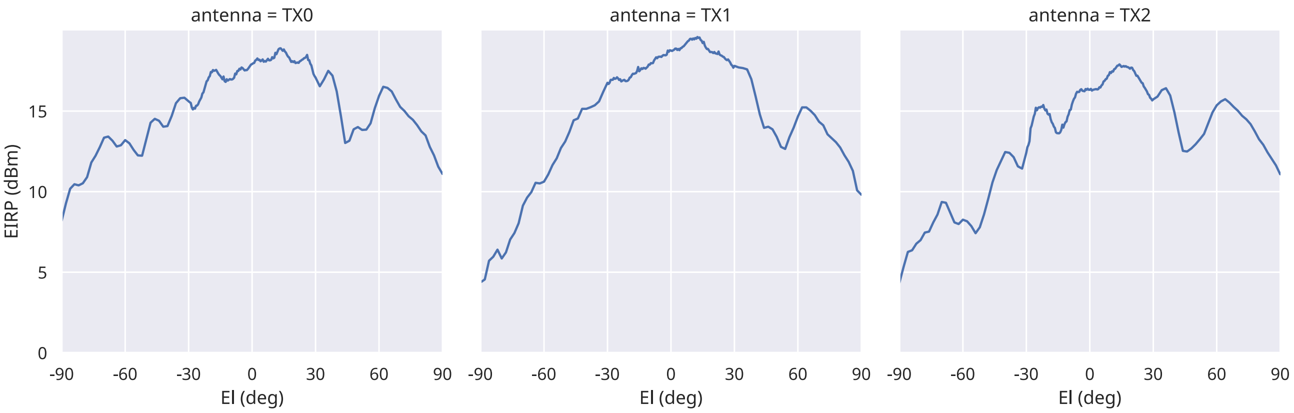


Figure 4: Typical E-plane EIRP (profile=1).

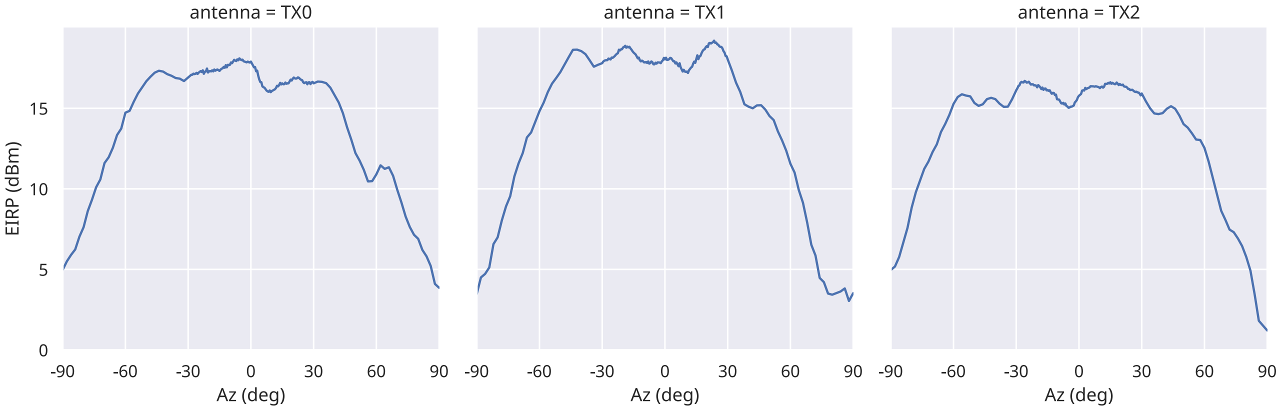


Figure 5: Typical H-plane EIRP (profile=1).

8.8. Thermal resistance characteristics

Table 15: Thermal resistance of A212 (on package).

Symbol	Parameter	Min	Typ	Max	Unit	Condition
θ_{jb}	Junction-to-board thermal resistance		34.2		°C/W	JEDEC JESD51-8
θ_{ja}	Junction-to-free-air thermal resistance		46.0		°C/W	JEDEC JESD51-2A v_{air}=0 m/s T_{op}=25°C power=360 mW

8.9. Distance standard deviation

Table 16 provides the distance standard deviation, defined as the standard deviation of the phase of the IQ samples.

Table 16: IQ sampling phase standard deviation (HWAAS=1, 50 frames, mean over channels).

Profile	T (°C)	Typ		Unit
		mean	std	
1	–40	2.0	0.2	deg
	25	1.9	0.2	deg
	85	2.1	0.2	deg
2	–40	2.0	0.2	deg
	25	2.0	0.2	deg
	85	2.1	0.2	deg
3	–40	2.1	0.3	deg
	25	2.1	0.2	deg
	85	2.3	0.2	deg
4	–40	2.2	0.3	deg
	25	2.2	0.2	deg
	85	2.4	0.2	deg
5	–40	2.3	0.3	deg
	25	2.4	0.2	deg
	85	2.7	0.2	deg
6	–40	2.4	0.3	deg
	25	2.4	0.2	deg
	85	2.7	0.2	deg

8.10. Distance estimation accuracy

The A212 sensor can estimate distance to objects using a detector application on top of the Radar System Software (RSS) library.

The typical trueness and precision of the distance detector delivered with the Acconeer Software Development Kit (SDK) is provided in Table 17.

Table 17: Mean of distance esitmation error absolute value (trueness) and standard deviation (precision). (T_{op} = 25 °C, nominal supplies, max trueness/precision of 99 tested devices).

Profile	T (°C)	Trueness	Precision	Unit
1	–40	11.4	0.3	mm
	25	11.6	0.4	mm
	85	11.2	0.5	mm
2	–40	14.3	0.4	mm
	25	14.3	0.4	mm
	85	12.7	0.8	mm
3	–40	17.4	0.8	mm
	25	15.6	0.9	mm
	85	14.3	1.3	mm
4	–40	21.3	0.9	mm
	25	19.0	0.9	mm
	85	18.8	1.4	mm
5	–40	39.0	1.7	mm
	25	30.7	1.6	mm
	85	26.2	3.1	mm

8.11. Angular estimation accuracy

The A212 sensor can be used to estimate the angle to objects using a detector application on top of the RSS library. The typical trueness and precision of the angular estimation detector delivered with the Acconeer SDK is provided Table 18.

Table 18: Mean of azimuth angle estimation error absolute value (trueness) and standard deviation (precision). (T_{op} = 25 °C, nominal supplies, conventional beamforming, max trueness/precision of 99 tested devices).

Profile	Elevation (deg)	Trueness	Precision	Unit
2	–20.0	1.8	1.4	deg
	0.0	2.4	1.4	deg
	20.0	2.7	1.6	deg
3	–20.0	1.8	1.5	deg
	0.0	2.3	1.5	deg
	20.0	2.7	1.7	deg

8.12. Radial resolution

The radial resolution gives the minimum measurable radial distance between two objects, and is defined in Table 19 as the Radial Full-Width-at-Half-Maximum Power (Radial FWHM Power) for the different profile configurations.

Table 19: Radial resolution for different profile configurations.

Profile	T (°C)	Typ		Unit
		mean	std	
1	–40	36.9	1.37	mm
	25	37.4	1.37	mm
	85	35.6	1.16	mm
2	–40	64.3	2.27	mm
	25	62.8	1.98	mm
	85	57.8	2.17	mm
3	–40	92.2	3.60	mm
	25	92.1	2.61	mm
	85	88.3	3.13	mm
4	–40	129.5	4.89	mm
	25	128.7	4.24	mm
	85	125.2	4.55	mm
5	–40	202.6	8.82	mm
	25	203.8	7.85	mm
	85	200.4	9.12	mm

8.13. Angular resolution

The angular resolution gives the minimum resolvable angular difference between two objects. It is a function of the virtual antenna array and the beamforming algorithm. In Table 20, the angular resolution is defined as the Angular Full-Width-at-Half-Maximum Power (Angular FWHM Power) for the different profile configurations.

Table 20: Angular resolution (conventional beamforming).

Profile	T (°C)	Typ		Unit
		mean	std	
1	–40	10.2	0.07	deg
	25	10.3	0.06	deg
	85	10.3	0.07	deg
3	–40	10.2	0.08	deg
	25	10.2	0.07	deg
	85	10.2	0.08	deg
5	–40	10.2	0.08	deg
	25	10.2	0.08	deg
	85	10.2	0.08	deg
6	–40	10.2	0.11	deg
	25	10.3	0.11	deg
	85	10.3	0.10	deg

8.14. Base Radar-Loop Gain (RLG)

The Radar-Loop Gain is a metric describing the sensitivity of the A212 sensor. It is based on the radar equation:

$$\mathrm{SNR}_{\mathrm{dB}} = 10 \cdot \log_{10}\left(\frac{P_{\mathrm{TX}} G_{\mathrm{TX}} G_{\mathrm{RX}} \lambda^2 \sigma \gamma}{(4\pi)^3 d^4 k T_s B}\right) \qquad \text{(Eq. 1)}$$

, where:

- P_{TX} is the transmit peak envelope power of the radar,
- G_{TX} is the TX antenna gain of the radar,
- G_{RX} is the RX antenna gain of the radar,
- λ is the wavelength of the radar,
- σ is the Radar Cross-Section of the target,
- γ is the reflectivity of the target,
- d is the radial distance to the target,
- k is the Boltzman constant,
- T_s is the system noise temperature of the radar,
- B is the bandwidth of the radar.

By grouping the constants and system-reladed parameters in the radar equation, it is possible to re-write it as:

$$\mathrm{SNR}_{\mathrm{dB}} = \mathrm{RLG}_{\mathrm{dB}} + \sigma_{\mathrm{dB}} + \gamma_{\mathrm{dB}} - 40 \cdot \log_{10}(d) \qquad \text{(Eq. 2)}$$

, from which we can express RLG as:

$$\mathrm{RLG}_{\mathrm{dB}} = \mathrm{SNR}_{\mathrm{dB}} - \sigma_{\mathrm{dB}} - \gamma_{\mathrm{dB}} + 40 \cdot \log_{10}(d) \qquad \text{(Eq. 3)}$$

RLG scales linearly with Hardware-Accelerated Average Sampling (HWAAS), with a 3 dB RLG increase for every doubling of HWAAS. Base RLG is defined as the RLG of the system when no HWAAS is performed (HWAAS=1).

Table 21: Base Radar-Loop Gain (RLG) for different profile configurations. (HWAAS=1, mean over channels, PRF = 20.8 MHz).

Profile	T (°C)	Typ		Unit
		mean	std	
1	–40	25.9	1.5	dB
	25	21.6	1.3	dB
	85	16.6	1.2	dB
2	–40	26.7	1.5	dB
	25	22.3	1.3	dB
	85	17.4	1.2	dB
3	–40	27.8	1.7	dB
	25	24.0	1.2	dB
	85	19.2	1.3	dB
4	–40	28.2	1.6	dB
	25	24.4	1.2	dB
	85	19.7	1.3	dB
5	–40	27.9	1.7	dB
	25	23.9	1.4	dB
	85	19.1	1.4	dB
6	–40	28.6	1.8	dB
	25	25.6	1.5	dB
	85	21.3	1.5	dB

8.15. Temperature sensor

The A212 radar sensor contains a temperature sensor used for keeping track of changes in the junction temperature (T_j). The absolute and relative accuracy of the temperature sensor is described in Table 22.

Table 22: Temperature sensor accuracy (nominal supplies, −40 °C ≤ T_{op} ≤ 85 °C).

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$T_{\texttt{bias-typ}}$	Typical temperature estimation trueness	−6.9		1.2	°C	
$T_{\texttt{std-typ}}$	Typical temperature estimation precision			3.0	°C	
$\Delta T_{\texttt{error}}$	Relative temperature estimation error		±3.9%			

9. Timing

9.1. Device start-up

9.1.1. DFU boot mode

Device Firmware Update (DFU) boot from the `UNPOWERED` state can be performed by asserting the `RESET_N` externally, as shown in Figure 6, or relying on the built-in power-on reset functionality, as shown in Figure 7. DFU boot by resetting the sensor from a powered state can be performed as described in Figure 8. Note that the `SPI0_SS_N` mode changes to from input with internal pull-up to output without any pull resistor when transitioning from DFU mode to executing the application. More information on the boot process is available on the *A212 Technical Reference Manual* provided with the A212 SDK.

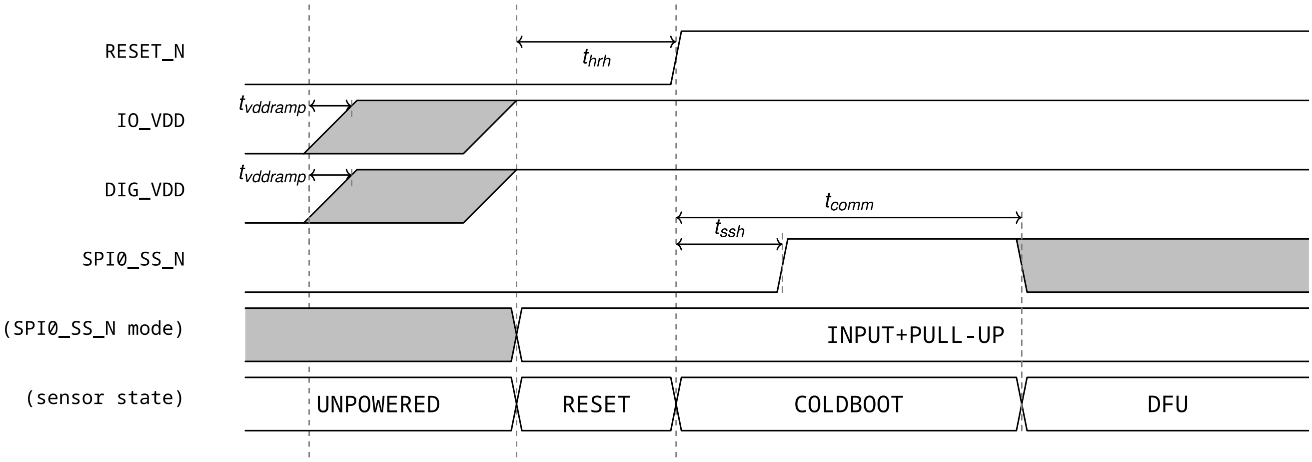


Figure 6: Device Firmware Update (DFU) boot in a configuration with a host-controlled RESET_N.

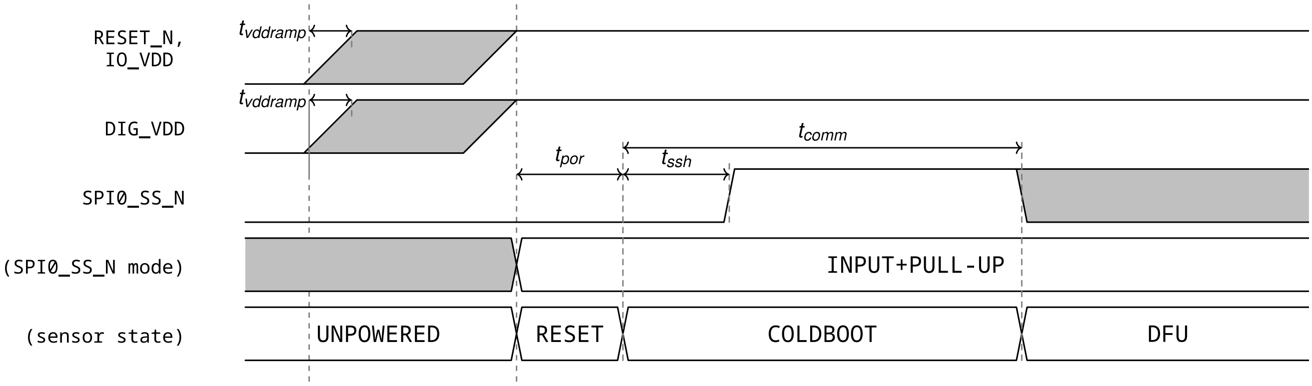


Figure 7: Device Firmware Update (DFU) boot in a configuration with RESET_N tied to `IO_VDD`.

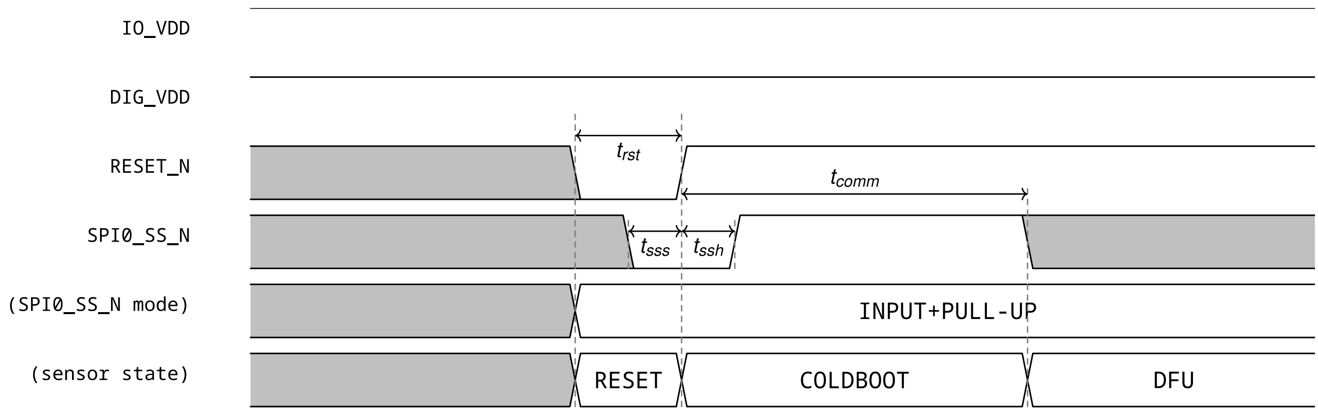


Figure 8: Device Firmware Update (DFU) boot by `RESET_N` assertion from a powered state.

Table 23: Device Firmware Update (DFU) boot timing parameters.

Symbol	Parameter	Min	Max	Unit	Condition
$t_{vddramp}$	IO_VDD and DIG_VDD ramp time	10		µs	
t_{hrh}	Host reset hold time	2600		µs	
t_{por}	Power-on reset time	480	2600	µs	
t_{rst}	Reset pulse time	10		µs	
t_{sss}	Slave-select setup time	1		µs	
t_{ssh}	Slave-select hold time	1	50 000	µs	
t_{comm}	DFU communication-ready time	100	120 000	µs	

9.1.2. NVM boot mode

NVM boot from the `UNPOWERED` state can be performed by asserting the `RESET_N` externally, as shown in Figure 9 or relying on the built-in power-on reset functionality, as shown in Figure 10. NVM boot by resetting the sensor from a powered state can be performed as described in Figure 11.

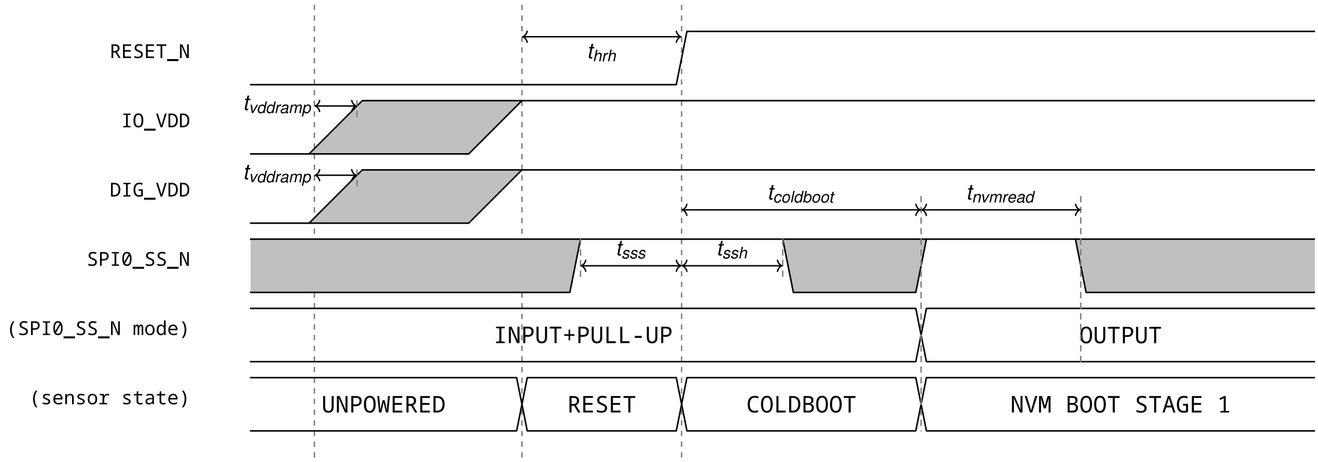


Figure 9: NVM boot in a configuration with a host-controlled `RESET_N`.

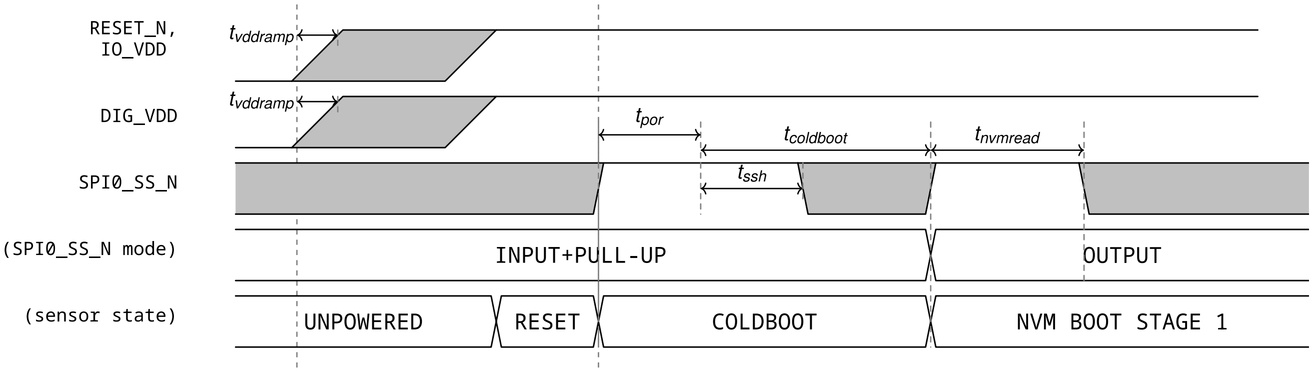


Figure 10: NVM boot in a configuration with RESET_N tied to IO_VDD.

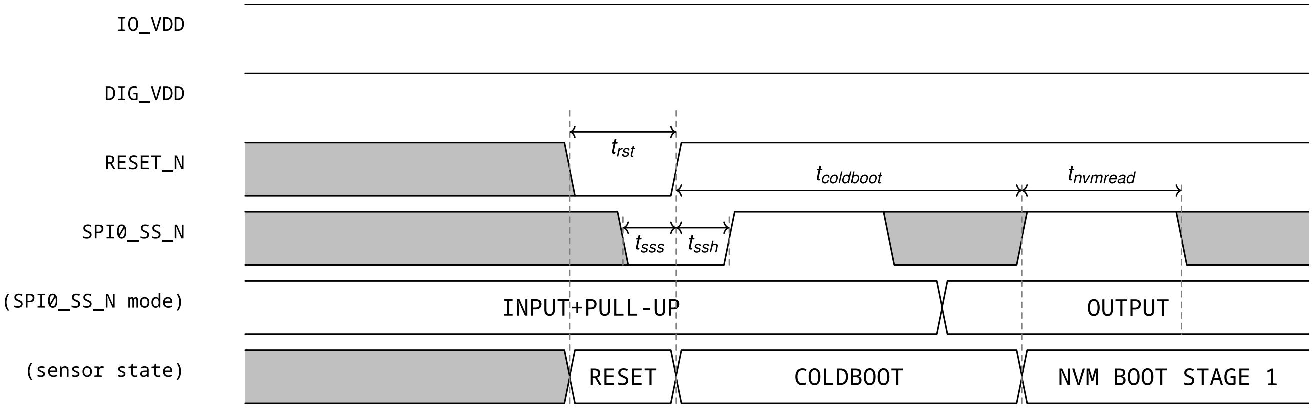


Figure 11: NVM by RESET_N assertion from a powered state.

Table 24: NVM boot timing parameters.

Symbol	Parameter	Min	Max	Unit	Condition
t_{vddramp}	IO_VDD and DIG_VDD ramp time	10		µs	
t_{hrh}	Host reset hold time	2600		µs	
t_{rst}	Reset pulse time	10		µs	
t_{sss}	Slave-select setup time	1		µs	
t_{ssh}	Slave-select hold time	1		µs	
t_{coldboot}	NVM access ready time		15 000	µs	
t_{nvmread}	NVM read ready time		200	µs	

9.2. SPI0

Figure 12 and Table 25 describe the timing specifications of the SPI0 (SPI0) interface. An overview of the key features of the interface is provdied in Section 10.1.2.

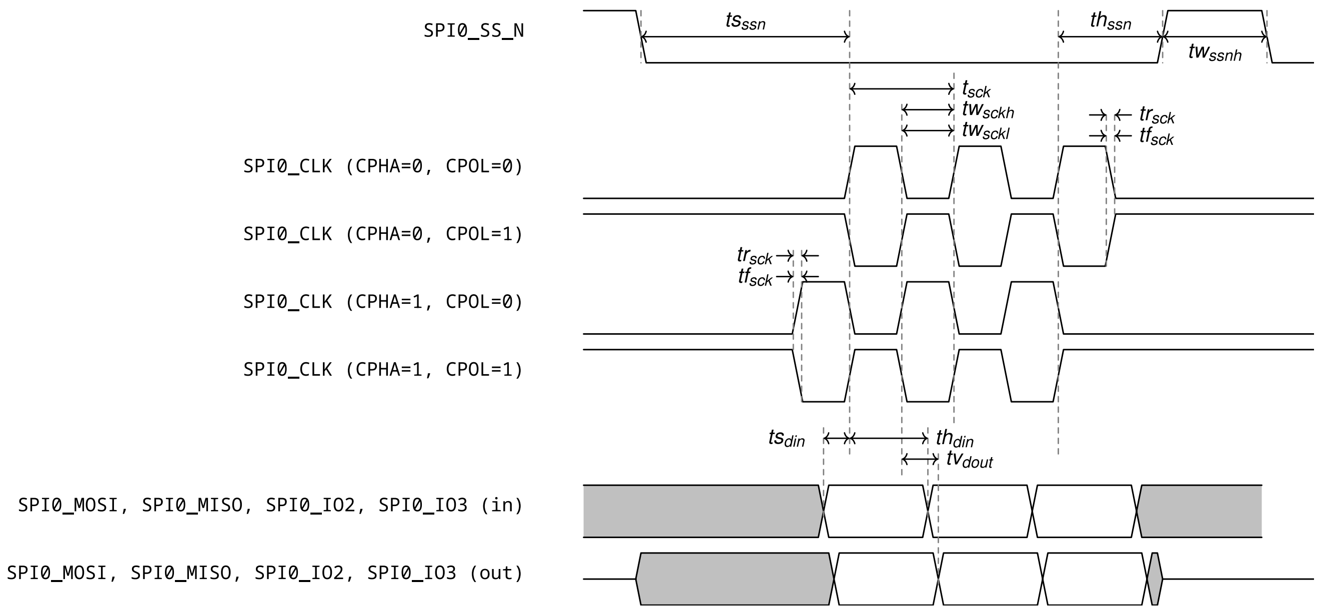


Figure 12: SPI0 timing diagram.

Table 25: SPI0 timing specification.

Symbol	Parameter	Master 3.3V		Slave 3.3V		Master 1.8V		Slave 1.8V		Unit	Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
ts_{ssn}	SPI0_SS_N setup time	10		10		10		10		ns	
th_{ssn}	SPI0_SS_N hold time	10		10		10		10		ns	
tw_{ssnh}	SPI0_SS_N high time	10		10		10		10		ns	
f_{sck}	SPI0_CLK clock frequency		47		50		47		50	MHz	No simultaneous transactions on the APPLICATION-SUBSYSTEM (APS) data buses.
t_{sck}	SPI0_CLK clock period	21		20		21		20		ns	
tr_{sck}	SPI0_CLK rise time		2		2		2		2	ns	$0.3V_{IO}$ to $0.7V_{IO}$; C_{load} = 30 pF
tf_{sck}	SPI0_CLK fall time		2		2		2		2	ns	
tw_{sckh}	SPI0_CLK high period time	10		10		10		10		ns	
tw_{sckl}	SPI0_CLK low period time	10		10		10		10		ns	
ts_{din}	Input data setup time	3		3		3		3		ns	
th_{din}	Input data hold time	2		2		2		2		ns	
tv_{dout}	Output data valid time		2		8		3		10	ns	C_{load} = 30 pF

More information regarding configuration of SPI0 and the structure of the transferred data can be found in the *A212 Sensor FW User Guide*, which is provided with the A212 SDK.

9.3. SPI1

Figure 13 and Table 26 describe the timing specifications of the SPI1 (SPI1) interface. An overview of the key features of the interface is provdied in Section 10.1.2.

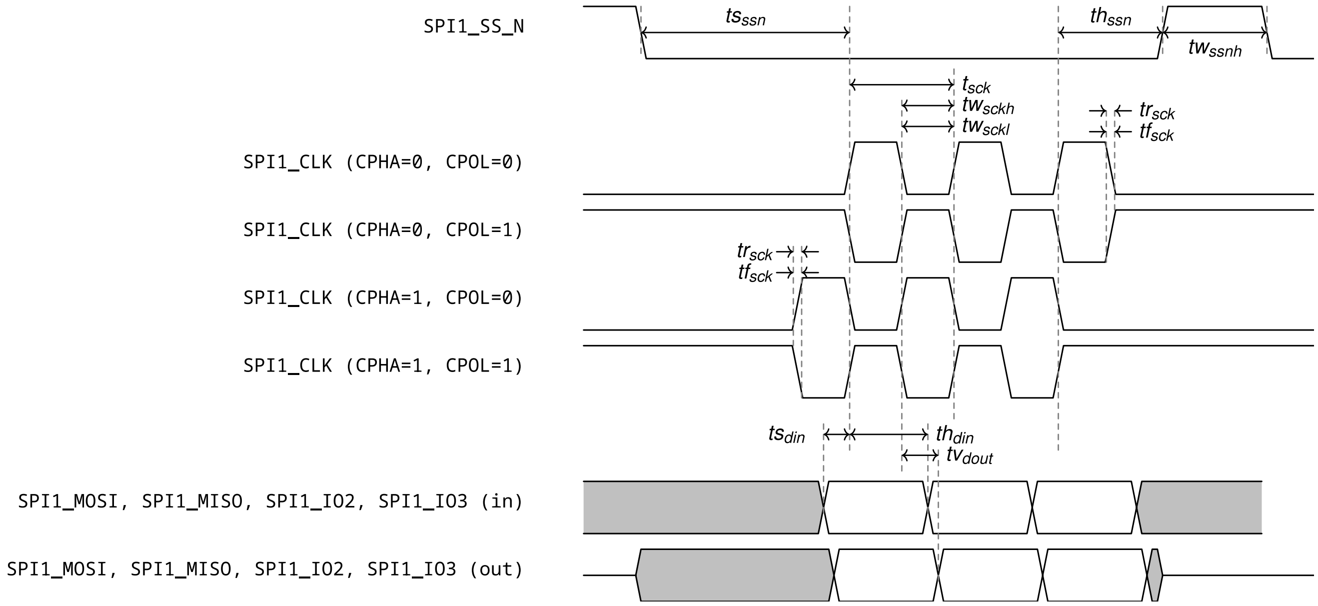


Figure 13: SPI1 timing diagram.

Table 26: SPI1 timing specification.

Symbol	Parameter	Master 3.3V		Slave 3.3V		Master 1.8V		Slave 1.8V		Unit	Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
ts_{ssn}	SPI0_SS_N setup time	10		10		10		10		ns	
th_{ssn}	SPI0_SS_N hold time	10		10		10		10		ns	
tw_{ssnh}	SPI0_SS_N high time	10		10		10		10		ns	
f_{sck}	SPI0_CLK clock frequency		47		50		47		50	MHz	No simultaneous transactions on the APS data buses.
t_{sck}	SPI0_CLK clock period	21		20		21		20		ns	
tr_{sck}	SPI0_CLK rise time		2		2		2		2	ns	$0.3V_{IO}$ to $0.7V_{IO}$; $C_{load} = 30$ pF
tf_{sck}	SPI0_CLK fall time		2		2		2		2	ns	
tw_{sckh}	SPI0_CLK high period time	10		10		10		10		ns	
tw_{sckl}	SPI0_CLK low period time	10		10		10		10		ns	
ts_{din}	Input data setup time	3		3		3		3		ns	
th_{din}	Input data hold time	2		2		2		2		ns	
tv_{dout}	Output data valid time		2		8		3		10	ns	$C_{load} = 30$ pF

More information regarding configuration of SPI1 and the structure of the transferred data can be found in the *A212 Sensor FW User Guide*, which is provided with the A212 SDK.

9.4. TWI

Figure 14, Figure 15, Figure 16 and Table 27 describe the timing specifications of the Two-Wire Interface (TWI) interface. An overview of the key features of the interface is provdied in Section 10.1.4.

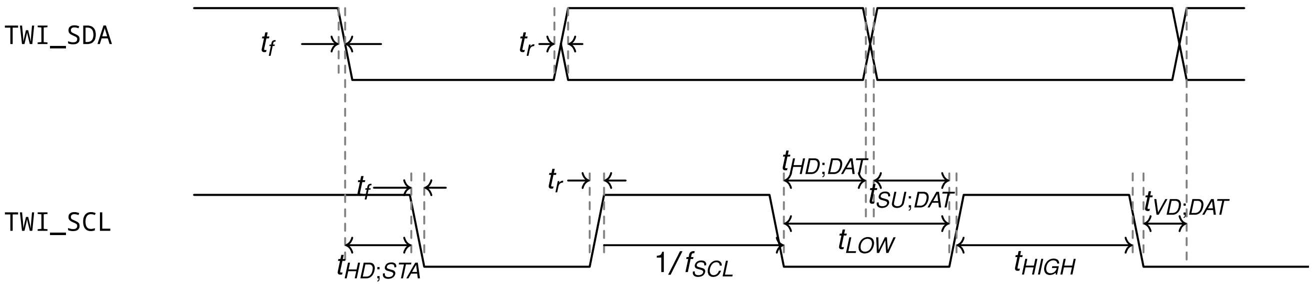


Figure 14: TWI data transfer timing diagram.

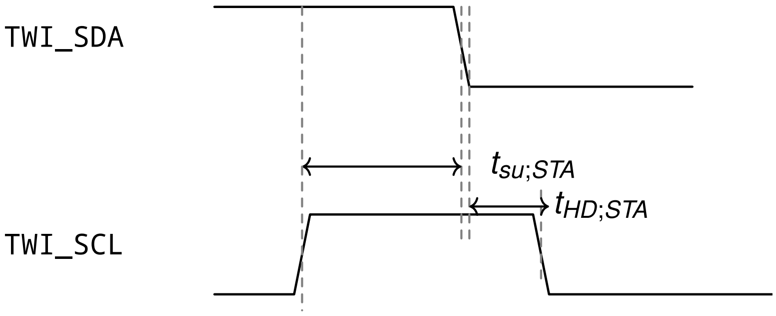


Figure 15: TWI start/repeat timing diagram.

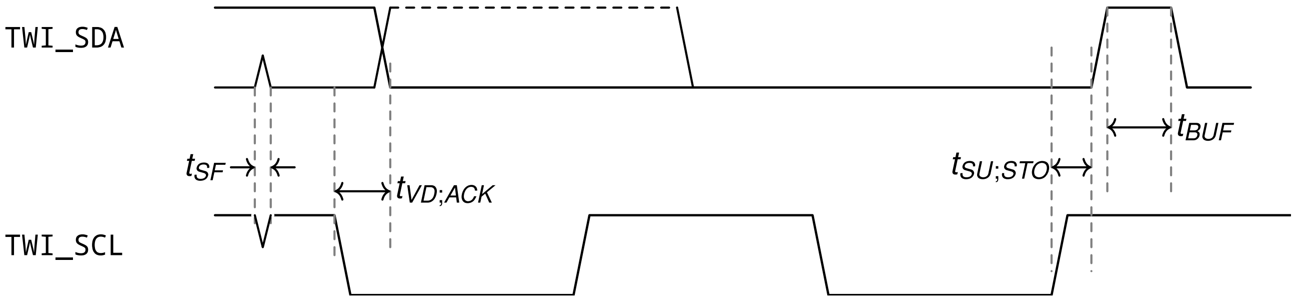


Figure 16: TWI ack/stop timing diagram.

Table 27: TWI timing specification.

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		50		50		50	ns	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz	
$t_{HD\text{-}STA}$	Hold time (repeated) START condition	4		0.6		0.26		µs	After this period, the first clock pulse is generated
t_{LOW}	Low period of the SCL clock	4.7		1.3		0.5		µs	
t_{HIGH}	High period of the SCL clock	4		0.6		0.26		µs	
$t_{SU\text{-}STA}$	Setup time for a repeated START condition	4.7		0.6		0.26		µs	
$t_{HD\text{-}DATA}$	Data hold time	0		0		0		µs	
$t_{SU\text{-}DATA}$	Data setup time	250		100		50		ns	
t_f	Fall time of both SDA and SCL signals		1000	$20 + 0.1C_b$	300		120	ns	
$t_{SU\text{-}STO}$	Setup time for STOP condition	4		0.6		0.26		µs	
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		0.5		µs	
C_b	Capacitive load for each bus line		400		400		550	pF	
$t_{VD\text{-}DATA}$	Data valid time		3.45		0.9		0.45	µs	
$t_{VD\text{-}ACK}$	Data valid acknowledge time		3.45		0.9		0.45	µs	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz	

10. Functional description

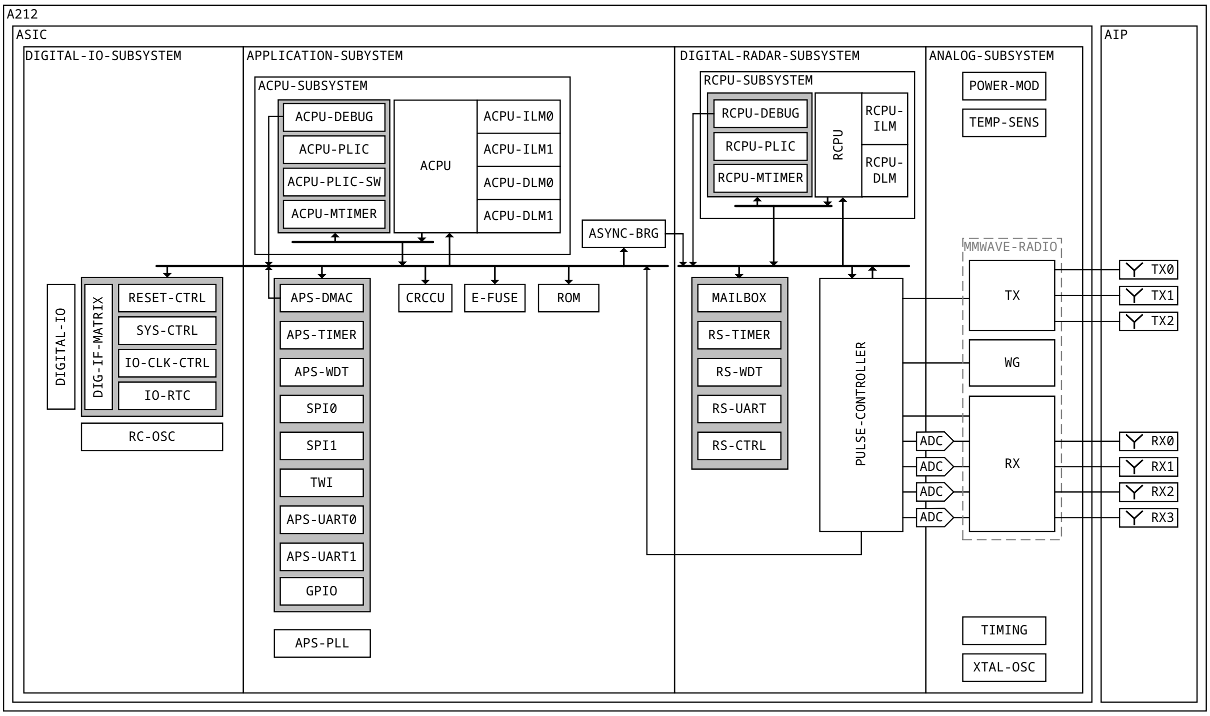


Figure 17: A212 functional block diagram.

10.1. Hardware

10.1.1. General purpose I/O (GPIO) interface

The A212 sensor features nine (9) General-Purpose Input and Output pins (`PIN0-PIN8`) These pins are highly configurable, supporting a wide range of functions including digital input, digital output, and various high-impedance states with programmable weak pull-up/pull-down resistors.

10.1.1.1. Key features

- **Multi-voltage I/O** - Supports 1.8V and 3.3V logic levels.
- **Programmable direction** - Each pin can be dynamically configured as an input, output, or high-impedance state.
- **Programmable drive strength** - Selectable output drive: 2 mA, 4 mA, 8 mA, or 12 mA.
- **Programmable slew rate** - Selectable between Fast and Slow slew rates for EMI control.
- **Programmable input hysteresis** - Optional Schmitt trigger input for improved noise immunity.
- **Programmable pull-resistors** - Configurable weak pull-up, pull-down, or bus-keeper (repeater) functionality.
- **Power-on safe state** - Pins have been configured to enter a defined state (High-Z, Pull-up, or Pull-down) during core power loss for system safety.
- **De-bouncing** - Input signals can be digitally low-pass filtered to eliminate bouncing.
- **Interrupt triggering** - Changes on the input signal can trigger SW interrupts.

10.1.1.2. Functional diagram

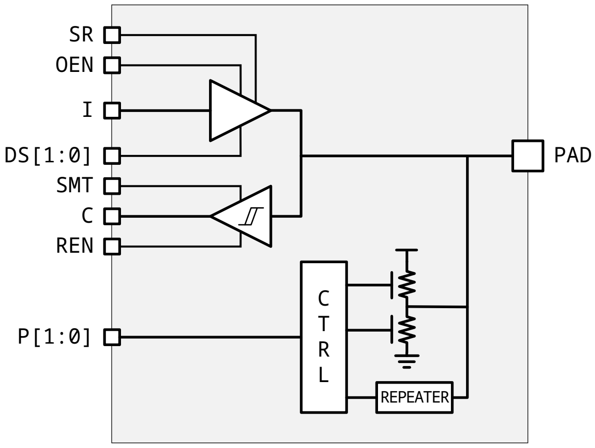


Figure 18: Digital I/O cell functional diagram.

Figure 18 provides a functional representation of the digital I/O cells connected to the `PIN0`-`PIN8` pins, where:

- PAD is connected to the corresponding sensor pin (`PIN0`-`PIN8`).
- `SR` configures the slew-rate.
- `OEN` enables the output buffer.
- `I` is the value driving the output buffer.
- `DS[1:0]` configures the drive strength.
- `SMT` configures the Schmitt trigger/hystheresis behavior of the input buffer.
- `C` is the detected logical value from the pad, which can be read by SW or configured to trigger interrupts, either directly or through a de-bouncing filter.
- `REN` enables the input buffer.
- `P[1:0]` configures the behavior of the pull-up / pull-down / repeater logic.

All the configuration signals above are memory-mapped onto SW-controlled registers. More information regarding how use the GPIO interface in SW is available on the *A212 Sensor FW User Guide*, provided with the A212 SDK.

10.1.1.3. Power-on start (POS) configuration

To ensure a safe state during power-up/power-down sequences, the configuration of the `PIN0` - `PIN8` has been configured as follows:

- `PIN4`, `PIN3` - These pins will be in a High-Z state if `IO_VDD` is supplied but `DIG_VDD` is not.
- All other pins (`PIN0` .. `PIN2`, `PIN5` .. `PIN8`) - These pins will be weakly pulled down if `IO_VDD` is supplied but `DIG_VDD` is not.

10.1.2. SPI0 and SPI1

The A212 sensor features two Serial Peripheral Interface (SPI) interfaces, named SPI0 and SPI1.

10.1.2.1. Key features

- Multi-voltage I/Os with programmable drive strength, slew rate, input hysteresis and pull-up/down resistors.
- Support for master and slave modes.
- Support for DSPI (only SPI0) and QSPI (only SPI0).
- Support of MSB/LSB first transfers.
- Support of Direct Memory Access (DMA) data transfers.

More information regarding configuration of SPI0 and SPI1 and the structure of the transferred data can be found in the *A212 Sensor FW User Guide*, which is provided with the A212 SDK.

10.1.3. UART0 and UART1

The A212 sensor features two Universal Asynchronous Receiver Transmitter (UART) interfaces, named UART0 (UART0) and UART1 (UART1), supporting full-duplex serial communication with configurable baud rates and data formats.

10.1.3.1. Key features

- Support of DMA data transfers.
- 16-byte transmit and receive FIFO buffers.
- Baud rate generation
  - Configurable divisor and oversampling ratio, resulting in support of baud rates from 9600 bps to 460 800 bps.
- Data format flexibility:
  - 5, 6, 7, or 8 bits per character.
  - 1, 1.5, or 2 stop bits.
  - Even, odd, stick, or no parity.
- Error detection:
  - Parity errors.
  - Framing errors.
  - Overrun errors.
  - Line break detection.
- Status reporting.
- Compatibility with industry-standard 16C550D UART.
- Hardware-based RTS/CTS flow control (UART0 only).

10.1.4. TWI

The A212 sensor features one TWI interface, implementing the standard features of the I2C bus protocol.

10.1.4.1. Key features

- Two-wire serial interface SDA + SCL.
- Open-drain / open-collector style signalling with external pull-ups.
- Programmable master and slave mode.
- 7-bit and 10-bit addressing, including *general call address*.

- Read/Write bit.
- ACK/NACK response.
- Start/stop conditions.
- Support for different speed modes:
  - Standard-mode (100 kb/s).
  - Fast-mode (400 kb/s).
  - Fast-mode Plus (1 Mb/s).
- Automatic clock stretching.
- Programmable clock/data timing.
- Support of DMA data transfers.
- Support for interrupts.

10.1.5. LIN

The A212 sensor features one Local Interconnect Network (LIN) interface. The LIN controller in APPLICATION-SUBSYSTEM is basically a UART with extra features to support the LIN slave mode.

10.1.5.1. Key features

- Slave mode support only.
- Header stage:
  - Hardware control.
  - Transition to response stage by break.
  - SYNC and PID reception.
- Response stage: Software control.
- Automatic baud rate adjustment by SYNC reception
- Supported baud rates: 2.4 kbps, 9.6 kbps, and 19.2 kbps.
- SYNC reception error detection and configurable behavior with optional interrupt generation.
- Interrupt generation upon PID reception (transition to response stage).
- PID parity or framing error detection and configurable behavior with optional interrupt generation.
- Header reception timeout detection with optional interrupt generation.
- Break reception interrupt during response stage. (software control; abort and transition to header stage)
- Termination of the response stage. (software control; transition to header stage)

10.1.6. SDP

The Serial Debug Port is a proprietary 2-wire debug interface from Andes Techology Corporation using the A212 pins `TCKC` and `TMSC`.

10.1.6.1. Key Features

- Configurable breakpoints.
- Support for system bus access.
- Support to interrupt generation, causing the processor to enter debug mode and redirect the instruction fetch to the debug exception handler.

10.1.6.2. Supported ICE hardware

To debug the A212 application software through the Serial Debug Port, an In-Circuit Emulation (ICE) device with support for the Andes Serial Debug Port protocol is required.

10.1.7. APPLICATION-SUBSYSTEM

The mission of the APPLICATION-SUBSYSTEM is to:

- Execute the application software, such as detectors based on the *Sparse IQ* data provided by the DIGITAL-RADAR-SUBSYSTEM (DRS).
- Communicate with an external host.
- Control the DRS.

The Application CPU (ACPU) is the RISC-V core at the centre of the APPLICATION-SUBSYSTEM. It is based on the N25F-SE IP from Andes Technologies and supports the RV32IMACF instruction set.

Table 28: Application CPU (ACPU) specifications.

Symbol	Parameter	Min	Typ	Max	Unit	Conditon
$f_{\texttt{acpu-high}}$	ACPU active-high clock frequency		286		MHz	
$f_{\texttt{acpu-mid}}$	ACPU active-mid clock frequency		26		MHz	
$f_{\texttt{acpu-low}}$	ACPU active-low clock frequency		32		kHz	
	ACPU instruction memory size		288		KB	
	ACPU data memory size		256		KB	

10.1.8. DIGITAL-RADAR-SUBSYSTEM

The mission of the DIGITAL-RADAR-SUBSYSTEM is to:

- Control the MMWAVE-RADIO and the TIMING blocks which are involved in sending and receiving radar pulses.
- Convert the data from the different radio channels into *Sparse IQ* data.
- Transfer the *Sparse IQ* data to the ACPU-DLM memory.

The software running on the DIGITAL-RADAR-SUBSYSTEM is provided as part of the SDK in the form of pre-compiled libraries. See Section 10.3 for more information.

10.1.9. ANALOG-SUBSYSTEM

The ANALOG-SUBSYSTEM holds the various analog blocks required for the A212 sensor such as internally regulated voltage supplies and low-jitter clocks. In addition, the ANALOG-SUBSYSTEM also contain the radio blocks.

10.1.9.1. POWER-MOD

POWER-MOD is responsible for regulating the supply `DIG_VDD` to internal voltage levels required for DIGITAL-IO-SUBSYSTEM, APPLICATION-SUBSYSTEM, and DIGITAL-RADAR-SUBSYSTEM. The supply `DIG_VDD` is specified in Section 8. POWER-MOD plays a key part in the implementation of the sensor states described in Section 10.4. The control of POWER-MOD is handled by drivers which are provided as part of the SDK. See Section 10.3 for more information.

10.1.9.2. TEMP-SENS

The A212 sensor is equipped with an integrated temperature sensor that can estimate the junction temperature. The TEMP-SENS data is accessed through a low-level driver provided as part of the SDK. See Section 10.3 for more information.

10.1.9.3. XTAL-OSC

The A212 sensor has a built-in crystal oscillator that generates a 26 MHz clock which is used both as system clock source and as radar reference clock. To function it requires external crystal components and further information on the component selection and requirements are described in Section 11.2. The XTAL-OSC has a separate supply `XO_VDD`, which is specified in Section 8.

10.1.9.4. TIMING

The A212 sensor is based on PCR technology and the system requires low-jitter clocks to collect the high-performance radar data. The TIMING block is responsible for generating low-jitter clocks for the radar and it is controlled by the software running on the DIGITAL-RADAR-SUBSYSTEM which is provided as part of the SDK in the form of pre-compiled libraries. See Section 10.3 for more information. TIMING has separate supplies, `ANA_VDD` and `VCO_VDD`, which are specified in Section 8.

10.1.9.5. MMWAVE-RADIO

The A212 sensor has got three transmit antennas and four receiver antennas, see Section 10.1.10 for more details on the antenna arrays. The three transmit antennas are connected to the TX block, which can be configured to select what outputs should transmit during the radar measurement. The four receiver antennas are connected to the RX block which contains a receiver and associated ADC for each antenna. The four receivers can be used simultaneously. The WG block generates a 60 GHz signal source for both TX and RX. The MMWAVE-RADIO subsystem is supplied by `TX_VDD`, `RX_VDD` and `WG_VDD`, which are specified in Section 8. MWAVE-RADIO is controlled by the software running on the DIGITAL-RADAR-SUBSYSTEM, which is provided as part of the SDK in the form of pre-compiled libraries. See Section 10.3 for more information.

10.1.10. AIP

Figure 19 shows the relative antenna position of transmit and receive antennas in the A212 package substrate.

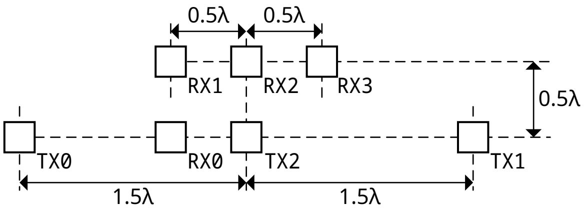


Figure 19: A212 physical antenna array.

Figure 20 shows the virtual antenna array derived from the physical placement of the antennas.

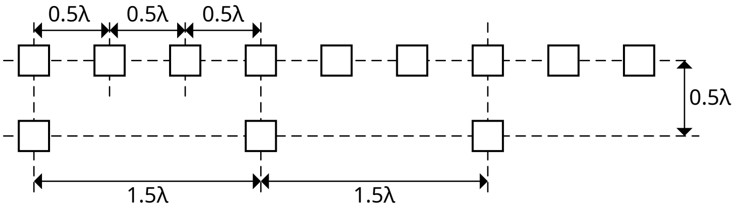


Figure 20: A212 virtual antenna array.

10.2. Boot process

The A212 sensor supports booting in the following modes:

- Normal Mode, in which the device boots from an NVM connected to the SPI0 interface.
- DFU mode, in which the A212 sensor allows an external host to transfer and execute firmware images via the SPI0 or UART0 interfaces.

If the sensor performs three consecutive restarts due to errors, it will enter an inactive operating mode known as Safe State.

These modes, as well as the boot process itself and the Safe State, are explained in detail in the *A212 Technical Reference Manual*, the *A212 NVM Image Format Application Note* and the *A212 DFU Protocol Application Note* provided with the A212 SDK.

10.3. Software

There are two ways to develop software for the A212 sensor. By using

- *Acconeer Sensor FW* or
- *User Sensor FW*.

10.3.1. Acconeer Sensor FW

When developing using *Acconeer Sensor FW*, all the software running inside the A212 sensor is provided by Acconeer. In this case, the protocol used to communicate with the software inside the A212 is clearly documented.

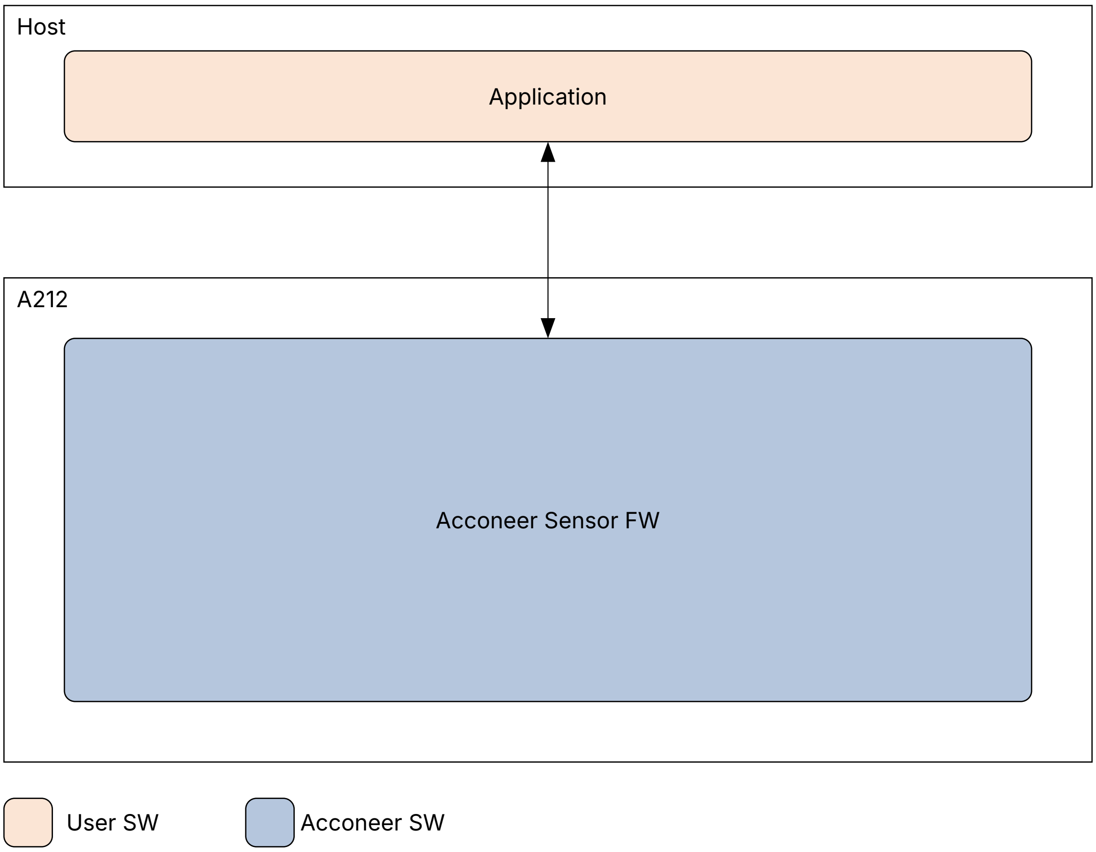


Figure 21: Acconeer Sensor FW architecture.

For further details, please see the *A212 Sensor FW User Guide* provided with the A212 SDK.

10.3.2. User Sensor FW

When developing using *User Sensor FW*, the software running inside the A212 sensor is developed by the user with the help of the RSS library, drivers, and examples provided by Acconeer.

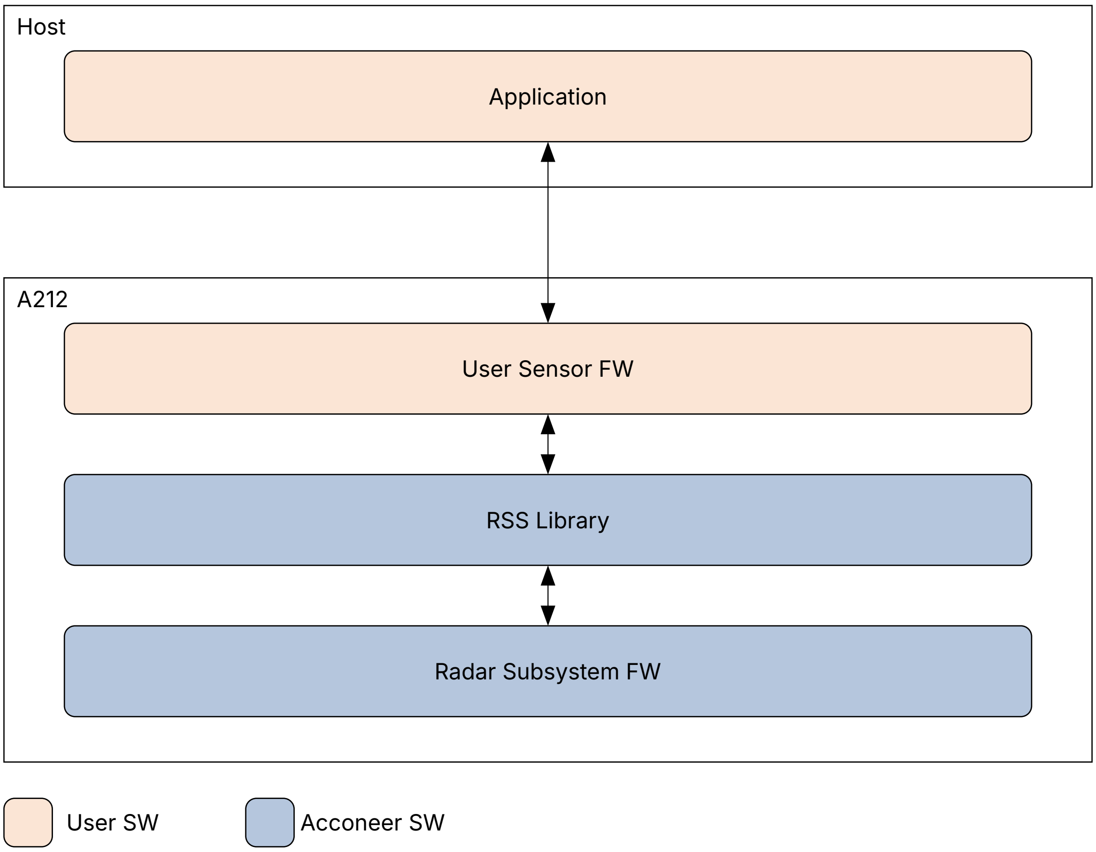


Figure 22: User Sensor FW architecture.

For further details, please see the *A212 Sensor FW User Guide* provided with the A212 SDK.

10.4. Sensor states

Table 29 defines some key sensor states that provide the reader with a representative view of the capabilities of the sensor.

Table 29: Simplified sensor state definitions.

Sensor state	Description	Memory retention	DIOS state	ACPU state	Radar state
`UNPOWERED`	No supplies applied.	None	Off	Off	Off
`SLEEP-ULTRA-DEEP`	Waiting to wake-up from internal timer or external interrupt.	None	On, 32 kHz	Off	Off
`SLEEP-DEEP`	Waiting to wake-up from internal timer or external interrupt.	Partial	On, 32 kHz	Off	Off
`SLEEP-SHALLOW`	Waiting to wake-up from internal timer or external interrupt.	Full	On, 32 kHz	Off	Off
`IDLE`	Waiting to wake-up from internal timer or external interrupt.		On, 32 kHz	WFI, 32 kHz	Off
`PROCESSING`	Data processing.		On, 26 MHz	Active, 286 MHz	Off
`MEASURE`	Measuring.		On, 26 MHz	WFI, 286 MHz	Active
`FULL`	Simultaneous measuring and processing.		On, 26 MHz	Active, 286 MHz	Active

10.5. Profiles

The A212 sensor can be configured to use six different sensor configurations, named *Profile 1* to *Profile 6*. *Profile 1* is optimized for maximum radial radial resolution and close-in range, while *Profile 6* is optimized for maximum Signal-to-Noise Ratio (SNR).

11. Integration

11.1. Power supplies

11.1.1. Supply schemes

The A212 sensor supports the supply schemes described in the below subsections.

11.1.1.1. Single 1.8 V supply

In this configuration, the A212 sensor is supplied by a single 1.8 V source connected to all supply input balls. See Figure 23 for further details.

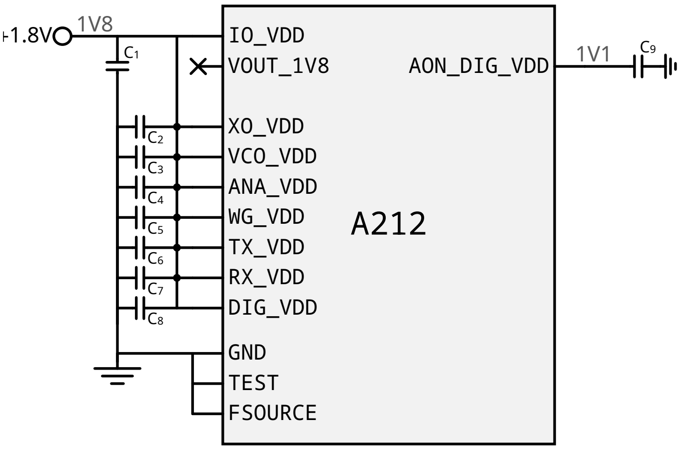


Figure 23: Single 1.8 V supply scheme.

11.1.1.2. Dual 3.3 V / 1.8 V supply

In this configuration, a 3.3 V source drives the `IO_VDD` balls, while a 1.8 V source drives the rest of the supply input balls. See Figure 24 for further details.

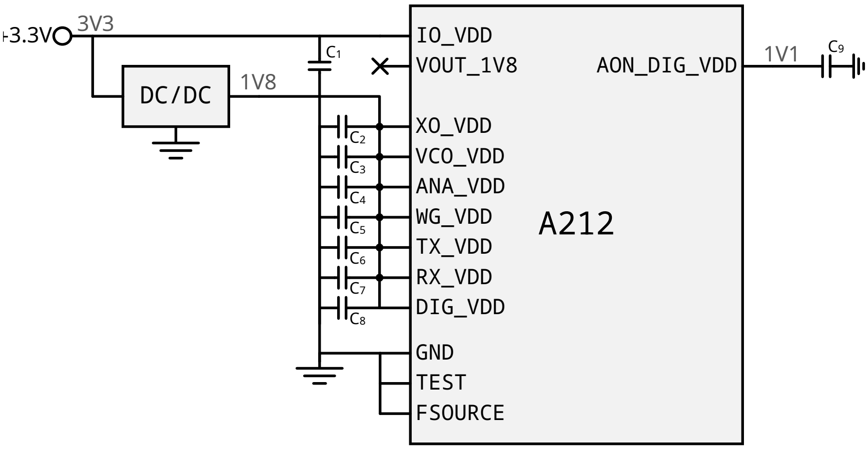


Figure 24: Dual 3.3 V / 1.8 V supply scheme with external DC/DC converter.

11.1.2. Supply noise

Noise in the power supplies may affect the performance of the A212 sensor. Table 13 provides the recommended maximum levels for the `DIG_VDD`, `RX_VDD`, `TX_VDD`, `WG_VDD`, `XO_VDD`, `VCO_VDD` and `ANA_VDD` supplies.

If the voltage source violates the supply ripple specifications in Table 13, an LC filter as displayed in Figure 25 can be used. This filter has a cut-off frequency of 23 kHz. The exact values for the LC filter depend on the frequency and amplitude of the ripple. Be aware of the LC filter peaking at the series resonance frequency $f = 1/\left(2\pi\sqrt{LC}\right)$. A small snubber resistor, 250 mΩ in the example filter, can be inserted to lower the Q factor.

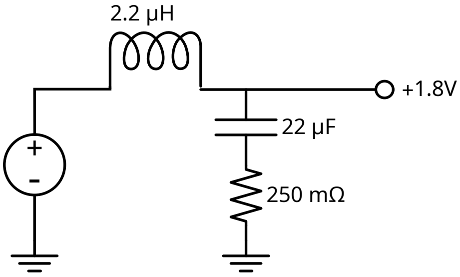


Figure 25: Optional LC supply filter.

11.2. XTAL

The A212 sensor has a built-in crystal oscillator that requires an external 26 MHz crystal (XTAL). For the oscillator to be able to drive the crystal, Eq. 4 needs to be fullfilled.

$$f_{xtal} \cdot C_L^{0.8} \cdot R_{ESR}^{0.61} < 0.7 \qquad \text{(Eq. 4)}$$

, where f_{xtal}, C_L and R_{ESR} come from the crystal datasheet and are defined in Table 31.

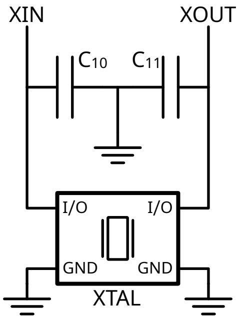


Figure 26: crystal (XTAL) connection diagram

Given the schematic in Figure 26, C_L can be calculated as described in Eq. 5.

$$C_L = \frac{C'_{10} \cdot C'_{11}}{C'_{10} + C'_{11}} \qquad \text{(Eq. 5)}$$

, where:

$$C'_{10} = C_{10} + C_{\text{10-parasitic}} \tag{Eq. 6}$$

$$C'_{11} = C_{11} + C_{\text{11-parasitic}} \tag{Eq. 7}$$

, where in turn:

- $C_{\text{10-parasitic}}$ is the Printed Circuit Board (PCB) trace and package capacitance between `XIN` and `GND`, which can expected to be between 1 pF and 2.5 pF.
- $C_{\text{11-parasitic}}$ is the PCB trace and package capacitance between `XOUT` and `GND`, which can also expected to be between 1 pF and 2.5 pF.

11.3. Digital interfaces

As described in Table 5, unused digital pins shall be connected to ground.

11.4. Other signals

11.4.1. `TEST` and `FSOURCE`

`TEST` and `FSOURCE` shall be connected to a solid ground plane.

11.5. BOM

Table 30: Bill of Materials (BOM).

Component	Value	Unit	Description
C_1	1	µF	De-coupling for `IO_VDD`.
C_2	1	µF	De-coupling for `XO_VDD`.
C_3	1	µF	De-coupling for `VCO_VDD`.
C_4	1	µF	De-coupling for `ANA_VDD`.
C_5	1	µF	De-coupling for `WG_VDD`.
C_6	1	µF	De-coupling for `TX_VDD`.
C_7	1	µF	De-coupling for `RX_VDD`.
C_8	1	µF	De-coupling for `DIG_VDD`.
C_9	1	µF	De-coupling for `AON_DIG_VDD`.
C_{10}	see Eq. 6		Tuning capacitance for XTAL, `XIN` side.
C_{11}	see Eq. 7		Tuning capacitance for XTAL, `XOUT` side.
R_1	33	Ω	Panic resistor to prevent damage in case of contention.
XTAL	26	MHz	Crystal.

Table 31: crystal (XTAL) electrical requirements.

Symbol	Parameter	Min	Typ	Max	Unit	Condition
f_{xtal}	Nominal frequency.		26		MHz	
$\varepsilon_{\mathrm{xtal}}$	Frequency tolerance.			±50	ppm	Including temperature stabilty.
C_L	Load capacitance.			see Eq. 4		See Section 11.2.
R_{ESR}	Equivalent series resistance.			see Eq. 4		See Section 11.2.

11.6. Typical integration scenarios

Figure 27 shows how the A212 sensor can be connected to an Microcontroller Unit (MCU). In this configuration the MCU will need to boot the A212 sensor in DFU mode, as per Section 9.1.1, and transfer the sensor firmware over the QSPI. The MCU can optionally use UART0 to receive logging information from the sensor.

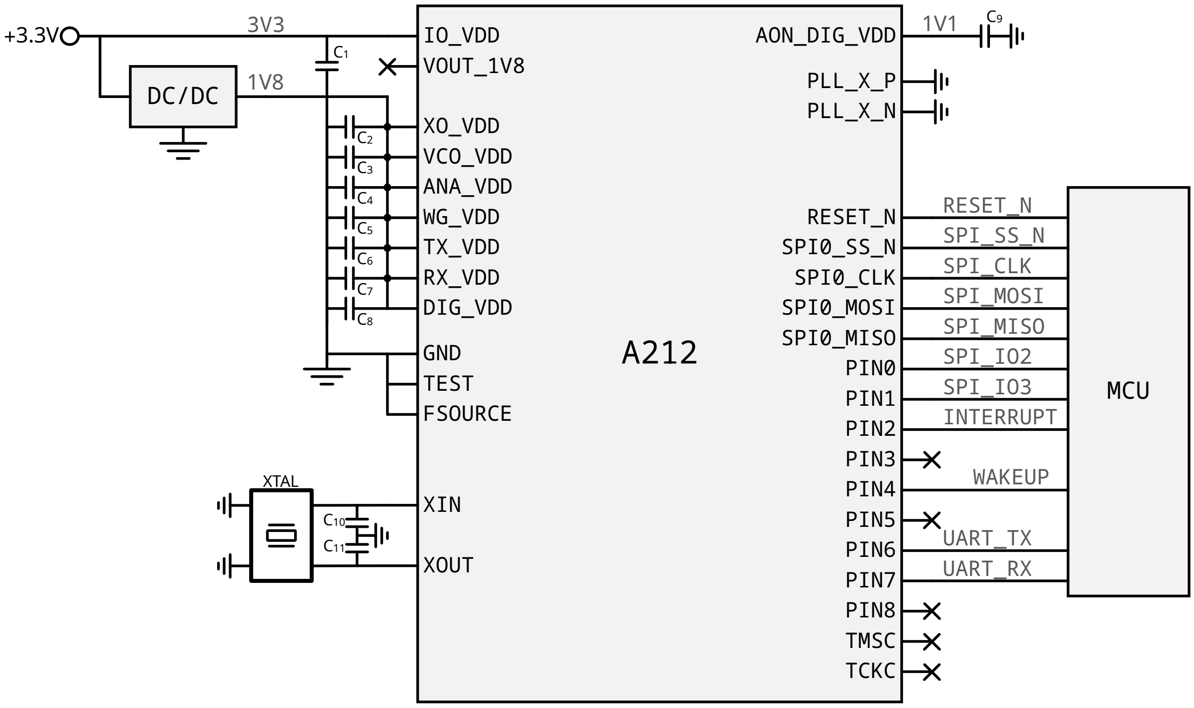


Figure 27: Integration example using dual 3.3V/1.8V supply and an external MCU.

Figure 28 shows how the A212 sensor can be connected to an NVM and an MCU. In this configuration the A212 sensor will boot in Normal Mode, described in the *A212 Technical Reference Manual*. The MCU is connected to the sensor using `PIN2` as interrupt, `PIN4` as wake-up pin and UART0 for data exchange.

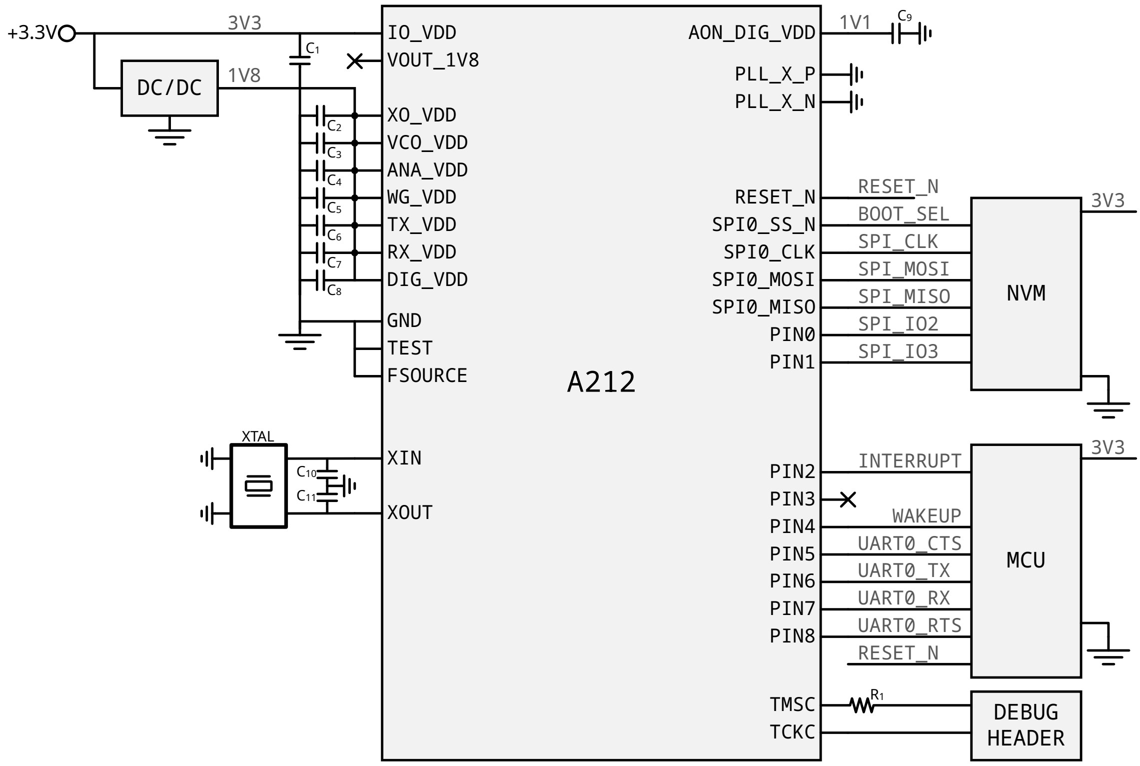


Figure 28: Integration example using dual 3.3V/1.8V supply, an Non-Volatile Memory (NVM) and an external MCU.

11.7. Layout recommendations

The sensor antennas are of folded dipole type, with their main ground reference being the internal package ground plane, extending below the whole area of the sensor. To further enhance the directivity of the sensor, the package ground plane should be extended by soldering all GND balls to the PCB top ground layer.

In terms of regulatory compliance, any openings in the ground plane inside the A212 footprint must be significantly smaller than the mmWave wavelength (5 mm in free space) to effectively shield off any disturbance. It is important to consider the PCB layout for optimal RLG performance. PCB layout guidelines can be found in the document “Hardware and Physical Integration Guidelines”.

12. Mechanical and marking specifications

12.1. Mechanical data

The A212 sensor is available in an Flip-Chip Chip-Scale-Package (fcCSP) package for mounting on a substrate. Table 32 below shows the mechanical properties.

Table 32: Mechanical data.

Parameter	Min	Typ	Max	Unit
Body X	16.85	16.90	16.95	mm
Body Y	5.80	5.85	5.90	mm
Body Z (height)		0.90	0.99	mm
Ball pitch	0.60	0.65	0.70	mm
Ball diameter	0.35	0.40	0.45	mm
Ball height	0.21	0.33		mm
Ball count		124		mm

The bottom view in Figure 29 shows the position of the 124 solder balls. The pitch of the BGA balls is 650 µm, the ball diameter is 400 µm and the collapsed ball height is 330 µm.

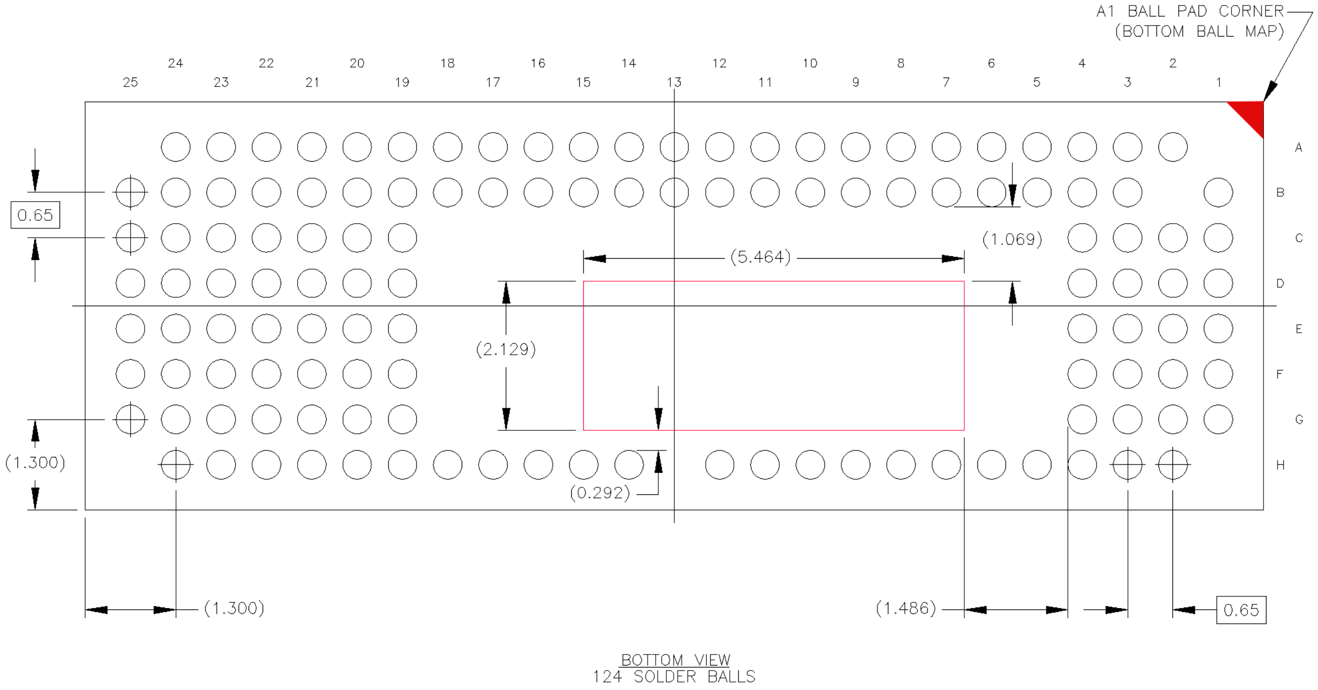


Figure 29: Physical layout of the A212 sensor, bottom view.

The package outline of the A212 sensor is shown in Figure 30 and Figure 31.

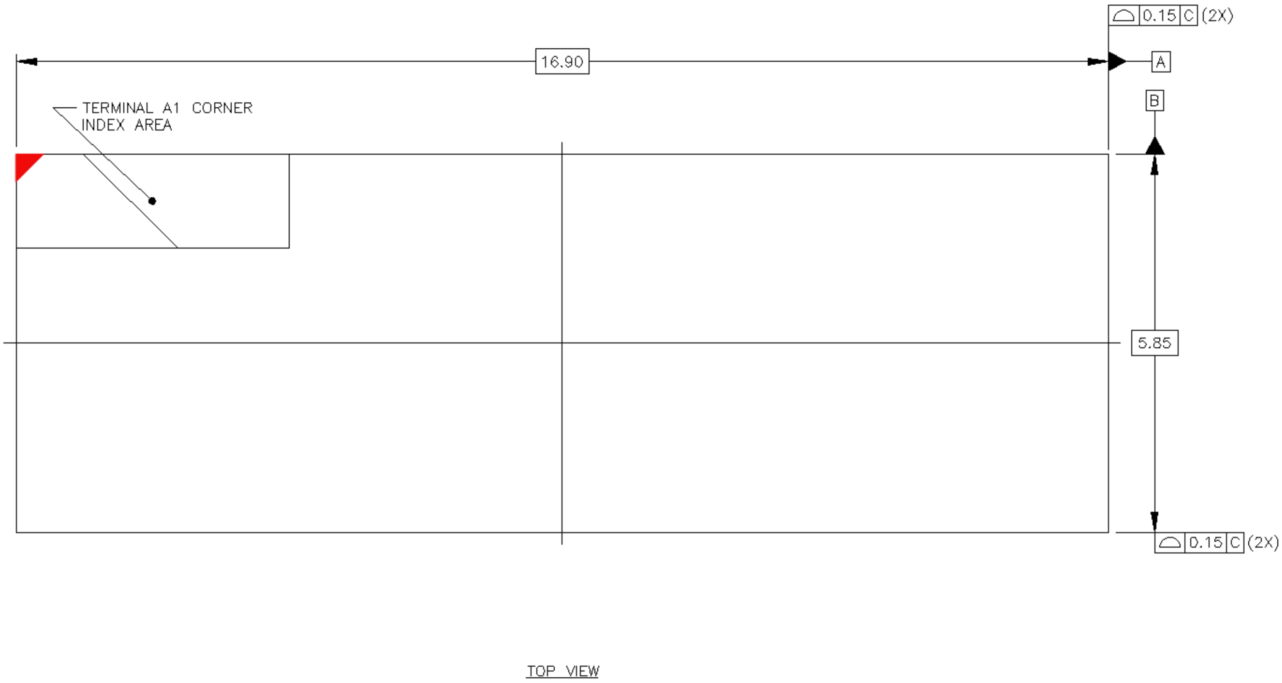


Figure 30: Package outline of the A212 sensor, top view.

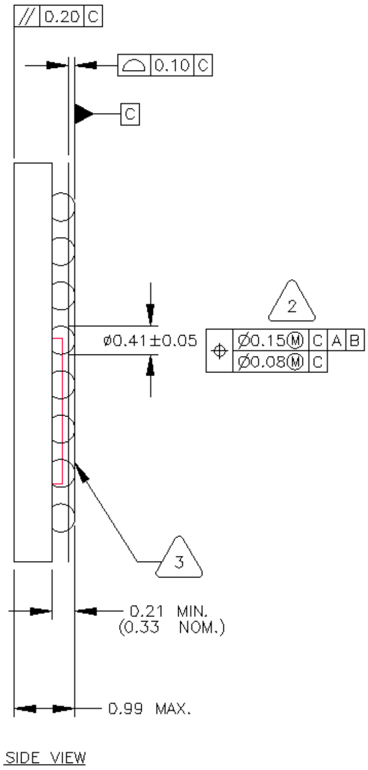


Figure 31: Package outline of the A212 sensor, side view.

Primary datum C and seating plane are defined by the spherical crowns of the solder balls. Dimension is measured at the maximum solder ball diameter, post reflow, parallel to primary datum C. All dimensions and tolerances conform to ASME Y14.5 – 2009.

12.2. Marking specification

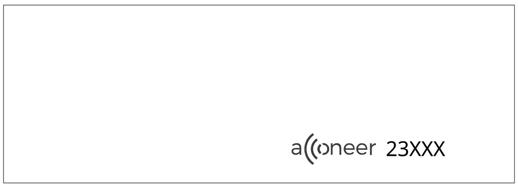


Figure 32: A212 consumer sensor marking.

The A212-003 sensors are marked with the Acconeer logo and a 5-character code as shown in Figure 32, where the two first characters are always “23” and denote the A212-003 product variant while the three last characters represent the lot number in hexadecimal format.

13. Handling

13.1. Moisture sensitivity level and recommended reflow profile

The Acconeer A212 sensor is a Moisture Sensitive Device (MSD) in accordance to the IPC/JEDEC specification. The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions. The A212 sensor is rated at MSL level 3. The maximum recommended number of reflow passes for A212 is 2. The A212 sensor has been qualified for reflow soldering and soldering heat resistance according to JEDEC J-STD-020, with “Preconditioning MSL 3: 30°C. 60%r.h., 192h”.

13.2. RoHS and REACH Statement

The A212 sensor meets the requirements of Directive 2011/65/EC of the European Parliament and of the Council on the Restriction of Hazardous Substances (RoHS) and the requirements of the REACH regulation (EC 1907/2006) on Registration, Evaluation, Authorization and Restriction of Chemicals.

14. Figures

15. Tables

16. Glossary

***ACPU* – Application CPU**: The RISCV core in APS.

***APS* – APPLICATION-SUBSYSTEM**: A digital subsystem in the A212 sensor.

***AiP* – Antenna-in-Package**: An integrated circuit (IC) packaging technology that combines an antenna with other radio frequency (RF) components and chips into a single package.

***DFU* – Device Firmware Update**: A boot mode of the A212 sensor.

***DIOS* – DIGITAL-IO-SUBSYSTEM**: A digital power domain in the A212 sensor.

***DMA* – Direct Memory Access**: A feature allowing peripherals to transfer data directly to/from the system memory.

***DRS* – DIGITAL-RADAR-SUBSYSTEM**: A digital subsystem in the A212 sensor.

***DSPI* – Dual Serial Peripheral Interface**: An SPI variant able to send 2 data bits per clock cycle.

***FIFO* – First-In First-Out**: A storage buffer where entries are read out in the same order they are stored.

***Angular FWHM Power* – Angular Full-Width-at-Half-Maximum Power**: Angular distance between the two points whose power is half the max power of the pulse.

***Radial FWHM Power* – Radial Full-Width-at-Half-Maximum Power**: Radial distance between the two points whose power is half the max power of the pulse.

***FoV* – Field of View**: Field of view. Since FoV is use-case dependent, in the context of this document it is defined as the azimuth and elevation $\mathrm{BW}_{-6\mathrm{dB}}$.

***GPIO* – General-Purpose Input and Output**: General-purpose digital interface pins.

***HWAAS* – Hardware-Accelerated Average Sampling**: Amount of samples per IQ point averaged in the sensor. HWAAS=1 means no averaging is performed.

***ICE* – In-Circuit Emulation**: The use of a hardware device or in-circuit emulator to debug the software of an embedded system.

***LIN* – Local Interconnect Network**: A low-cost communication protocol primarily used in automotive applications, designed to connect various electronic components.

***MCU* – Microcontroller Unit**: Integrated Circuit (IC) including one or more processor cores, memory and input/output peripherals.

***NVM* – Non-Volatile Memory**: External memory that can be connected to the A212 sensor through the SPI0 interface.

***PCB* – Printed Circuit Board**: A laminated sandwich structure of conductive and insulating layers.

***PCR* – Pulsed Coherent Radar**: A patented radar technology from Acconeer.

***QSPI* – Quad Serial Peripheral Interface**: An SPI variant able to send 4 data bits per clock cycle.

***RCS* – Radar Cross-Section**: A metric describing how well a target reflects the radar signal depending on its shape and size.

***RLG* – Radar-Loop Gain**: A metric derived from the radar equation that describes the sensitivity of the radar for a given configuration.

***RSS* – Radar System Software**: A pre-compiled library with radar control software provided with the A212 SDK.

***SDK* – Software Development Kit**

***SDP* – Serial Debug Port**: Andes Technology Corporation's proprietary 2-wire serial deug port interface.

***SNR* – Signal-to-Noise Ratio**: A measure comparing the strength of a desired signal to background noise.

***SPI* – Serial Peripheral Interface**: A standard interface for serial communications.

***SPI0* – SPI0**: The primary SPI interface of the A212 sensor, with support for quad throughput.

***SPI1* – SPI1**: The secondary SPI interface of the A212 sensor.

***TWI* – Two-Wire Interface**: A synchronous, multi-master/multi-slave, single-ended, serial communication bus compatible with the I2C protocol.

***UART* – Universal Asynchronous Receiver Transmitter**: A peripheral device for asynchronous serial communication in which the data format and the transmission speeds are configurable.

***UART0* – UART0**: A UART interface of the A212 sensor, which is used for logging during boot.

***UART1* – UART1**: A UART interface of the A212 sensor.

***XTAL* – crystal**: A piezoelectric crystal used as a frequency-selective element in an electronic oscillator circuit.

***Base RLG* – Base Radar-Loop Gain**: RLG for a configuration in which HWAAS is set to 1. This provides a normalized metric for the system sensitivity.

***fcCSP* – Flip-Chip Chip-Scale-Package**: A semiconductor packaging technology that uses flip-chip bonding and is characterized by its small size.

DISCLAIMER

The information herein is believed to be correct as of the date issued. Acconeer AB ("Acconeer") will not be responsible for damages of any nature resulting from the use or reliance upon the information contained herein. Acconeer makes no warranties, expressed or implied, of merchantability or fitness for a particular purpose or course of performance or usage of trade. Therefore, it is the user's responsibility to thoroughly test the product in their particular application to determine its performance, efficacy and safety. Users should obtain the latest relevant information before placing orders.

Unless Acconeer has explicitly designated an individual Acconeer product as meeting the requirement of a particular industry standard, Acconeer is not responsible for any failure to meet such industry standard requirements.

Unless explicitly stated herein this document Acconeer has not performed any regulatory conformity test. It is the user's responsibility to assure that necessary regulatory conditions are met and approvals have been obtained when using the product. Regardless of whether the product has passed any conformity test, this document does not constitute any regulatory approval of the user's product or application using Acconeer's product.

Nothing contained herein is to be considered as permission or a recommendation to infringe any patent or any other intellectual property right. No license, express or implied, to any intellectual property right is granted by Acconeer herein.

Acconeer reserves the right to at any time correct, change, amend, enhance, modify and improve this document and/or Acconeer products without notice.

This document supersedes and replaces all information supplied prior to the publication hereof.

Acconeer AB
Västra Varvsgatan 19
211 77 MALMÖ
Sweden

www.acconeer.com
info@acconeer.com
+46 10 218 92 00