Replacing A111 with A121

1 Table of Contents

2 Revision History

Revision	Comment
v 1.0	First released version
v 1.1	Added information regarding A121 crystal resonance frequency requirement (Added chapter 4, “Crystal resonance frequency”.
v 1.2	Updated chapter 4 “Crystal resonance frequency”.
v 1.3	Updated typo in Figure 4.

3 Introduction

The A121 Pulsed Coherent Radar Sensor shares PCB layout footprint with the A111 Pulsed Coherent Radar Sensor but encompasses a lot of new functionality and features. **The A121 sensor can be mounted onto an existing PCB for the A111 without any layout updates**, **given that the existing A111 HW Integration includes a crystal with resonance frequency 24MHz.** It is however possible to improve the BOM cost if the PCB layout is updated. Note that the software libraries and software APIs have been updated and applications must be updated or rewritten for the A121.

4 Crystal resonance frequency

As can be seen in Figure 1 and Figure 2 where the A111 and A121 recommended HW Integrations at 1.8V are shown, both A111 and A121 require an external crystal (X1) to be able to operate:

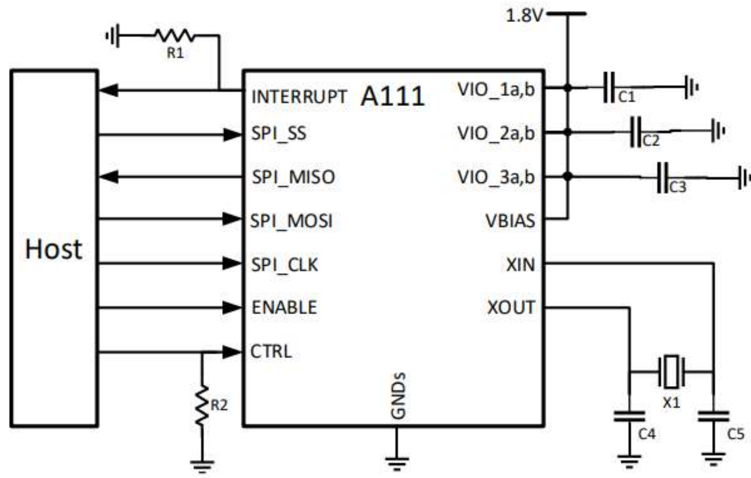

Figure 1 The A111 recommended HW integration.

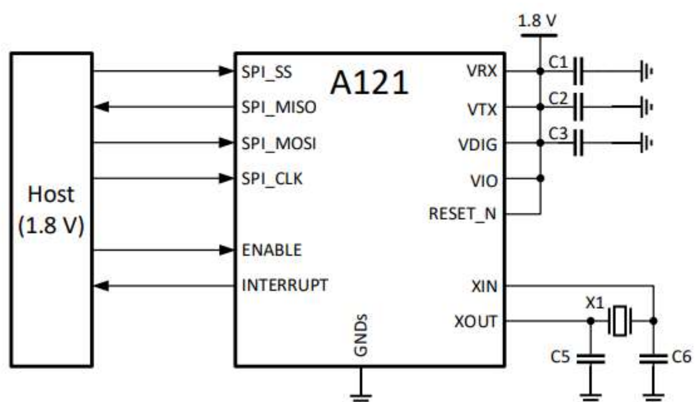

Figure 2 The A121 recommended HW integration when connected to a host MCU running at 1.8V.

For details regarding the component values in above figures, refer to A111 and A121 datasheets [1], [2].

The A121 only supports a crystal with resonance frequency of 24MHz, as opposed to A111 that also supported other frequencies. In A121 SW it is not possible to configure the frequency of the input clock.

5 BOM optimization when replacing A111 with A121

5.1 Removal of power switch

If you have a power switch to cut off the voltage supply to VIO1 and VIO2 when the ENABLE signal is low in your A111 HW integration, this component can be removed for the A121. The reason is that the leakage current of VRX and VTX of A121 is less than 1 µA when the ENABLE signal is low (compared to ~66 µA for A111 VIO1 and VIO2). Figure 3 shows what the integration might look like for A111. Figure 4 shows what the integration with A121 could look like.

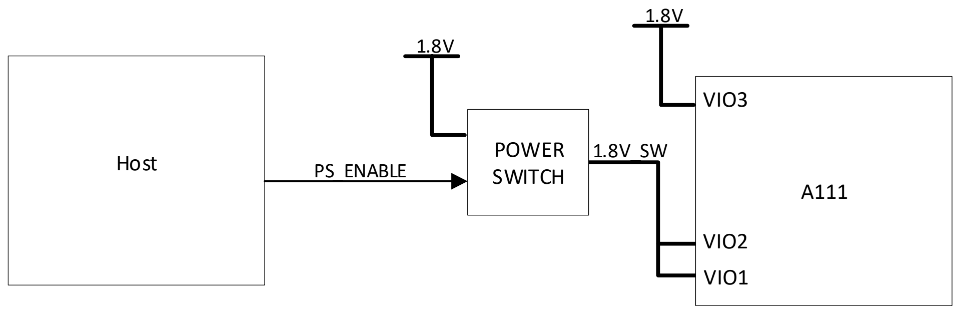

Figure 3. Power supply integration of the A111 with a power switch to minimize leakage currents of VIO1 and VIO2 when ENABLE signal is low. PS_ENABLE is the enable signal of the power switch.

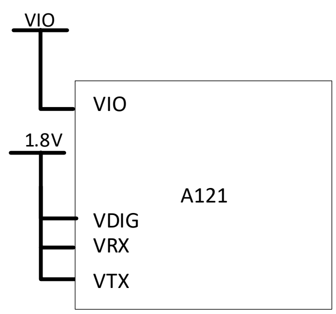

Figure 4. Power supply integration of the A121 for minimizing the leakage current of VRX and VTX when ENABLE signal is low. For VIO = 1.8 V, VIO can be connected to the same 1.8 V power domain as VDIG, VRX, VTX.

5.2 Removal of level-shifter

If your host MCU is operating at another voltage than 1.8 V, your A111 hardware integration includes a level-shifter circuit to convert the SPI and GPIOs for 1.8 V operation. The A121 VIO power domain can however be supplied by either 1.8 V or 3.3 V and therefore the SPI and GPIOs of the A121 can be connected directly to the host MCU without the need for a level shifter.

Figure 5 shows a block schematic of an A111 HW integration using a bidirectional level-shifter circuit. Figure 6 shows the A121 HW integration where no level-shifting circuit is needed.

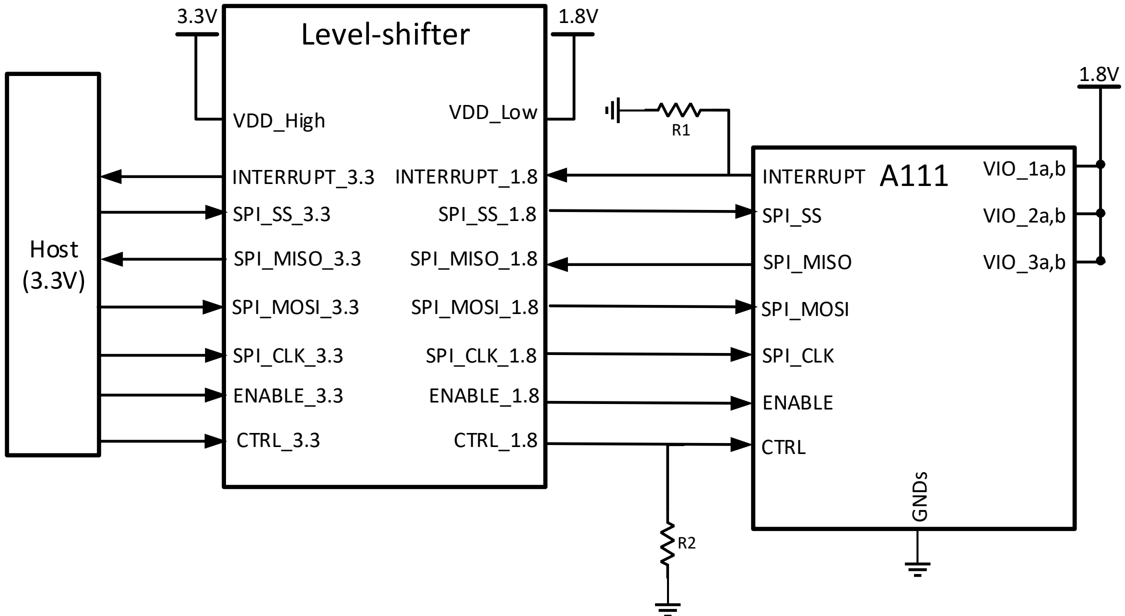

Figure 5. Example A111 integration with a 3.3 V host MCU using a bidirectional level-shifter.

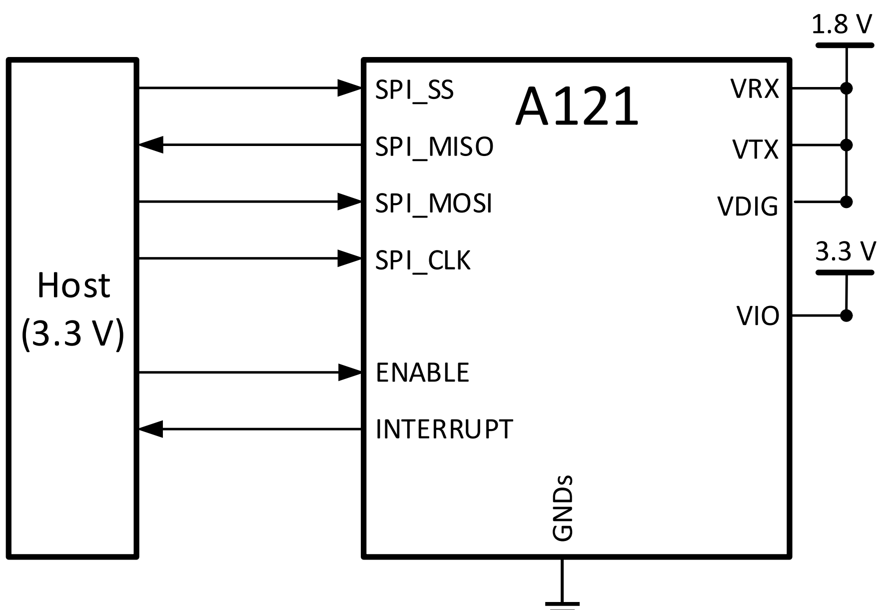

Figure 6. An example of A121 integrated with a 3.3 V host MCU.

6 Optimizing the ground plane

6.1 Remove CTRL signal

The CTRL signal is not needed for A121 to exit hibernate state and this signal can thus be removed. Refer to Figure *1* and Figure *2* for details on the recommended HW Integration of A111 and A121. If A121 is simply replacing A111 in an already existing PCB layout, it is important that pin A9 “CTRL” is always held low. If not used in A121 or A111, CTRL should be connected to ground. For details regarding A121 recommended HW integration when connected to a host MCU running at 3.3 V, refer to the A121 datasheet [2].

6.2 Connect pins A2 and B1 to ground

In A111, the A2 and B1 pads must be left unconnected to ensure proper operation of the radar sensor. In A121, these pads can be either unconnected or connected to ground. To optimize the ground plane of the A121, it is recommended to connect these pins to ground. The green circle in Figure 7 shows the difference in ground plane when these pins are unconnected (left-hand side picture) and connected to ground (right-hand side picture). The blue circle shows the CTRL pin A9 breaking up the ground plane in the left-hand side picture. In A121 (right-hand side picture), CTRL is connected to ground.

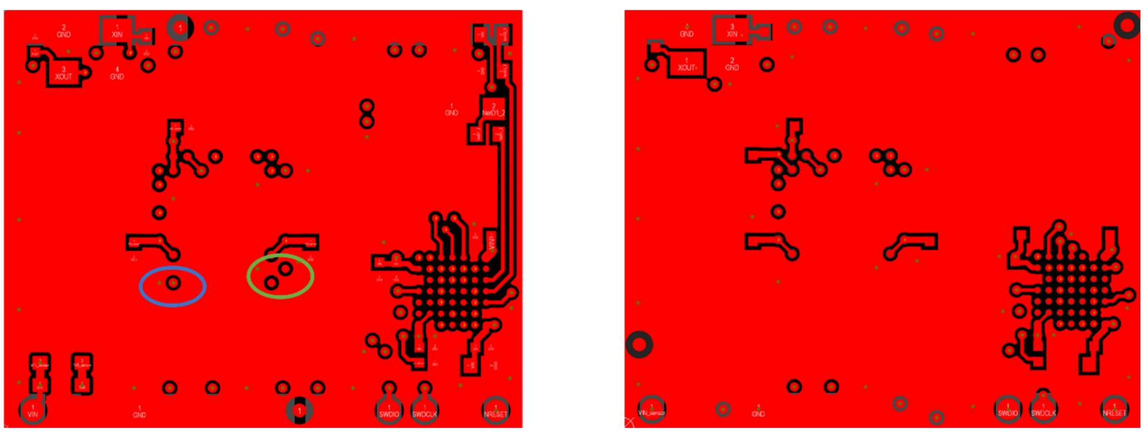

Figure 7. The top layer ground plane of the XM124 module with A111 (left) and XM125 with A121 (right).

7 References

[1] A111 datasheet: https://developer.acconeer.com/download/a111-datasheet-pdf/

[2] A121 datasheet: https://developer.acconeer.com/download/a121-datasheet-pdf/

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